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Fabrication and Characterization of Manhattan Style Josephson Junctions for Superconducting Quantum Bits

MASTER THESIS

by

Julian Daser

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UNIV.-PROF. DR. GERHARD KIRCHMAIR

Abstract

Josephson junctions build the backbone of superconducting quantum circuits. The resonance frequency of a qubit is directly related to the nonlinear inductance introduced by the Josephson effect. As thickness and area of the tunnel barrier set the physical properties of the junction, the qubit parameters can be engineered over a wide range. This design flexibility comes at the cost of reproducibility, as the dimensions heavily rely on the fabrication parameters.

So far qubit fabrication in the Innsbruck cleanroom facilities has been limited by predictability and reproducibility of the junction parameters. To optimize the fabrication, Manhattan style Josephson junctions were adopted, as recent studies promise stable results. To investigate this fabrication recipe 38 chips of Al/AlOx/Al Manhattan junction test devices were fabricated on 3 wafers containing a total of 7182 junctions. To study the influence of fabrication parameters on junction properties 4 different sets of oxidation parameters and 9 different junction areas were realized. Characterization of the junction uniformity is performed by measurement of room temperature resistance. The average standard deviation for junctions on the same chip is below 3%. An average global spread over all test devices of 10% was obtained. This spread seems to be dominated by junction area variations resulting from variations in the electron beam lithography.

To validate the room temperature measurements 18 X-mon qubits were characterized in a waveguide configuration. The standard deviation for qubits with the same target frequency is on average below 1.6%.

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Mama & Peter, Papa & Astrid - Danke!

Contents

We here present an approach to the calculation of tunnelling currents between two metals that is sufficiently general to deal with the case when both metals are superconducting. In that case new effects are predicted due to the possibility that electron pairs may tunnel through the barrier leaving the quasiparticle distribution unchanged.
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(i) At finite voltages the usual DC current occurs, but there is also an AC super current of amplitude $|J_1|$ and frequency $2 \cdot e \cdot V/\hbar$.

(ii) At zero voltage J_0 is zero, but a DC supercurrent of up to a maximum of $|J_1|$ can occur.

(B.D. Josephson, 1962)

CHAPTER 1

Introduction

In 1962 *B.D. Josephson* changed the understanding of physics by predicting the coherent tunneling of Cooper pairs between two superconductors coupled by a weak link [1]. Due to Cooper pair tunneling the DC Josephson effect (ii) engenders the flow of a supercurrent across the weak link without an existing potential difference between the superconductors. If a DC voltage is applied across the weak link, the AC Josephson effect (i) leads to an alternating supercurrent. A physical implementation of a weak link is a superconductor-insulator-superconductor (SIS) junction, also called Josephson junction. In 1963 *P. W. Anderson* & *J. M. Rowell* were the first to observe the Josephson effect in their SIS junction experiment [2]. The Josephson effect is a macroscopic quantum phenomenon that can introduces non-linearity without dissipation or dephasing [3]. Integrating Josephson junctions into electrical circuits the unique properties of the Josephson effect can be harnessed.

The idea of processing information with a quantum computer was first proposed by *Richard Feynman* in 1981 [4]. Since then the field of quantum information has progressed rapidly. Superconducting quantum circuits are one of the leading platforms in the development of fault tolerant quantum processors [5–8]. They consist of superconducting capacitors and inductors that form local microwave oscillators. Making the circuits superconducting circumvents dissipation.

The backbone of superconducting quantum bits are Josephson junctions. The nonlinear inductance introduced to the circuit by the Josephson effect allows for the oscillators to be anharmonic. This way a non-degenerate, atom like, energy spectrum with addressable transitions is formed. Thus superconducting quantum bits are often referred to as artificial atoms [5]. In comparison to naturally occurring atoms their physical properties can be engineered by circuit parameters which offers high flexibility. This flexibility though comes at the cost of reproducibility. A natural atom has an intrinsic frequency that is the same for each of its kind. Superconducting circuits are man-made devices consisting of billions of atoms. The precision one can predict

the frequency of a superconducting circuit previously to measuring it is an engineering challenge.

Since the realisation of the first superconducting qubit in 1999 [9], the main focus of design engineering was set to increasing coherence times [7, 10]. With more and more qubits in one device the need for better reproducibility and predictability has come up to avoid problems such as cross talk [11, 12]. Although it is the smallest element of the circuit the Josephson junctions have a great influence on reproducibility. The nonlinear inductance introduced by the junctions is directly linked to the resonance frequency. This inductance is determined by the area and thickness of its insulating barrier. Both parameters are set by the fabrication and thus are tuneable, which introduces variability. There have been reports of successful post fabrication junction barrier annealing [13]. But scaling up to thousands of qubits will require further improvements in fabrication.

Josephson junctions can be fabricated using different materials and techniques. Shadow evaporation of $Al/AlO_x/Al$ junctions has become the de-facto standard for superconducting qubits. So far the *Innsbruck Circuits* research group has been using the bridge free junction technique [14]. Using this approach the reproducibility and predictability of qubit frequencies have varied up to 50%, making it difficult to scale up. Recent studies have shown that Manhattan style junctions promise high reproducibility [11, 15, 16]. During this masters thesis Manhattan Style Josephson Junctions were fabricated for the first time in the Innsbruck clean-room. After optimizing the fabrication process test devices have been fabricated to characterize the reproducibility of the newly implemented junctions. Fabricating junctions of different barrier size and thickness will allow to predict resonance frequencies over a wide range in the future. As the normal state resistance of a Josephson junction is proportional to its inductance [17], the junctions can be characterized by resistance measurements at room temperature.

In addition to the room temperature measurements X-mon (transom) qubits [18, 19] have been fabricated and characterized to validate the room temperature measurements and calibrate the fabrication process. Determination of the proportionality constant between resistance and inductance, the so-called superconducting gap, will further improve predictability.

The thesis is organized in the following way. In chapter 2 a basic introduction into nanofabrication techniques is given. The challenges and limitations one may face from fabrication will be pointed out. Chapter 3 begins with a theoretical description of Josephson junctions. Afterwards different junction fabrication techniques are compared and the benefits of Manhattan junctions will be discussed. The chapter ends with the detailed fabrication steps of the junction test devices. Characterization of the room temperature devices will be discussed in chapter 4. This is followed by a detailed analysis of the statistics obtained. In chapter 5 a short introduction into transmon qubits is given and design, simulation and fabrication of the qubits with the Manhattan junctions will be explained afterwards. Chapter 6 includes the characterization of the qubits followed by a short analysis. The thesis ends with a conclusion and outlook in chapter 7.

CHAPTER 2

Nanofabrication

As discussed in the introduction, superconducting circuits are man-made quantum devices. The process of building a superconducting circuit is called nanofabrication as the smallest features go down to the nanometer scale. At these length scales dust particles are bigger than the fabricated structures, thus fabrication has to be done in a very clean environment. Such environments are called clean rooms. Fabrication for this master thesis was carried out at the *Quanten Nano Zentrum Tirol (QNZT)* that is shared between the *Institute for Quantum Optics and Quantum Information* and the *University of Innsbruck*. Below an introduction into the key fabrication techniques is given. This introduction is influenced by questions and problems I encountered. I hope future clean room users can benefit from reading it.

2.1 Chemicals

There are a few chemicals that are used repeatedly in fabrication processes. Below, some of their chemical properties are mentioned and it is pointed out why they are useful.

Acetone is a colorless organic compound with the chemical formula C_3H_6O. Acetone is a volatile liquid at room temperature and ambient pressure, with a boiling point of 56.2 °C. Heating Acetone one has to be very careful as acetone vapor is highly flammable. Due to its low molecular weight and simple structure, it evaporates quickly and is highly soluble in water. The evaporation coefficient of Acetone is 2. A higher evaporation coefficient means the solvent is less volatile [20]. It is an excellent solvent for many organic compounds including polymers. This qualifies acetone as a cleaning agent for substrates and it is used for various lift-off processes. As acetone is known to leave residues it should never be the last chemical used in any fabrication step.

Isopropanol (IPA) is a clear, colorless liquid at room temperature with the chemical formula C_3H_8O. IPA has a boiling point of 82.6 °C and a evaporation coefficient of 11. IPA is known for its excellent organic solvent properties and is used to clean and remove contamintion from

samples and equipment. IPA is also used as a developer in combination with water. Pure IPA does not develop or dissolve resist.

Ethanol, also known as ethyl alcohol, is a clear, colorless, and flammable liquid with the chemical formula C_2H_5OH. The boiling point of Ethanol is at 78.37°C and it has an evaporation coefficient of 8.3. Ethanol is a universal solvent used for cleaning and degreasing surfaces, electronics, and machinery.

DI-water, short for deionized water, has had almost all of its ions removed, resulting in a highly purified form of water. It is used in applications where the presence of minerals, ions, or impurities in water can be problematic. DI-water is the cleanest solvent in the clean room and is produced by an in-house DI water machine. It is used for cleaning and chemical purposes. DI-water has an evaporation rate of 80, making it the solvent that is the hardest to remove from a substrate.

2.2 Substrates

A substrate provides the surface on which circuits are build on. There are different materials and sizes of substrates available. At *QNZT* silicon and sapphire wafers with 2-inch diameter and a thickness of 275 nm and 330 nm respectively are used. Both substrates show one of the lowest available dielectric loss tangents [21, 22]. The advantage of sapphire is the very high resistivity but it has the disadvantage of needing a discharge layer for e-beam lithography and can only be diced by a laser or a diamond saw. Silicon comes in different resistivity classes, the prime wafers that are used have a resistivity of $10 - 100$ kΩcm^2. The substrates should be cleaned previous to fabrication which will ensure that previous handling will have no influence on the fabrication. For test devices this can be done using acetone and IPA baths in combination with sonication while for qubits the substrates are cleaned with a piranha solution. Piranha is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). Piranha cleaning is known to increase the coherence time of qubits [10]. Due to the danger that comes with handling the strong acid it is only used when necessary. For a detailed study of the state of the art substrate cleaning the reader is referred to Ref. [23].

2.3 Spin Coating

Photoresists are the second ingredient of an fabrication process. They form the mask for further subtractive or additive steps. Resists consist of organic compounds whose solubility is changed by the impact of high energy photons or electrons. Spin coating is a common technique to obtain well controlled resist film thicknesses on a substrate. A detailed discussion can be found in Ref. [24]. At *QNZT* commonly homogeneity and reproducibility with less than 5% variation in film thickness are achived using a *Suess Microtec LabSpin6*.

To coat the substrates they are placed on a rotary vacuum chuck that can be fully enclosed by a lid. A few ml resist are dispensed on the substrate which is afterwards brought to rotation with typical speeds between 1000-8000 rpm. The centrifugal force introduced by the rotation evenly spreads the dispensed resist on the substrate. Excess resist is spun off the edge of the substrate. As the solvent starts to evaporate during the spinning the thinning of the resist film decreases with time until it comes to a stop. The final resist film thickness depends on time,

acceleration and speed of the spinning process with the latter being the main contributor. Thus resists come with a certain range of attainable film thickness. This range is strongly depending on the residual solvent content. The manufacturer of the resist usually provides a data sheet with some values that can be used as a reference. For critical processes the exact spinning parameters have to be calibrated.

A common problem of spin coating is the formation of an edge bead due to surface tension leading to a significantly increased resist height. To circumvent this effect fabrication is done on 2 inch wafers and the circuit layout is placed with some distance to the edge. Spinning on small or rectangular substrates is not recommended as edge bead effects increase. Although homogeneity is better than 5% there is a trend of decreasing film thickness towards the edge (neglecting the edge bead). This effect results from the increased rotational speed moving further away from the rotational axis.

Spinning is the process where one has to care most about a clean substrate. Every particle will destroy the spinning process as it changes the flow direction of the resist. The spinning area is thus designed to have the lowest particle concentration in the clean room. When spinning resist I wipe every critical area with IPA before starting the process. After that I make sure there is no clean room wipe left in the spinning area to avoid pieces of fluff and ensure good laminar flow of air. When the sample is on the vacuum chuck of the spinner I blow on it with a N_2 gun multiple times. From thereon I try to stay as well as possible behind the rubber curtain to not introduce any particles.

The resists are filled in small bottles so that the large storage bottles have smaller likelihood to be contaminated. It is good practice to filter resists. While most people store their resist in a fridge I keep my bottles at room temperature to ensure a stable viscosity. The pipette used to dispense the resist should be clean, and I therefor carefully blow it with a N_2 gun before its use. To prevent the formation of air bubbles in the film I do not dispense the full content from the pipette.

When spin coating is done the wafer is transferred to a hotplate for a soft bake. During the soft bake the remaining solvent evaporates and the resist hardens out. The time and temperature of the soft bake are resist and process specific. The height of a resist film can be checked optically after soft baking by using an ellipsometer. The resist manufacturer provide the so called Cauchy coefficients that are resist specific. At *QNZT* a *Horiba SmartSE* ellipsometer is available, where individual substrate and resist stack models can be fitted. Multiple resist films can be spun on top of each other to harvest the properties of different resist types or to achieve increased thicknesses. This way three-dimensional mask shapes can be formed. Soft bake parameters for the lower layers might have to be adapted in case of a stack.

2.4 Lithography

The circuit layout is imprinted into the resist film by a patterning exposure. Depending on the resist this can be done either by electron-beam or photo lithography. The impinging electrons or photons interact with the resist and change its chemical properties. There are two interaction types of resists called positive tone and negative tone. A schematic of their working principle is

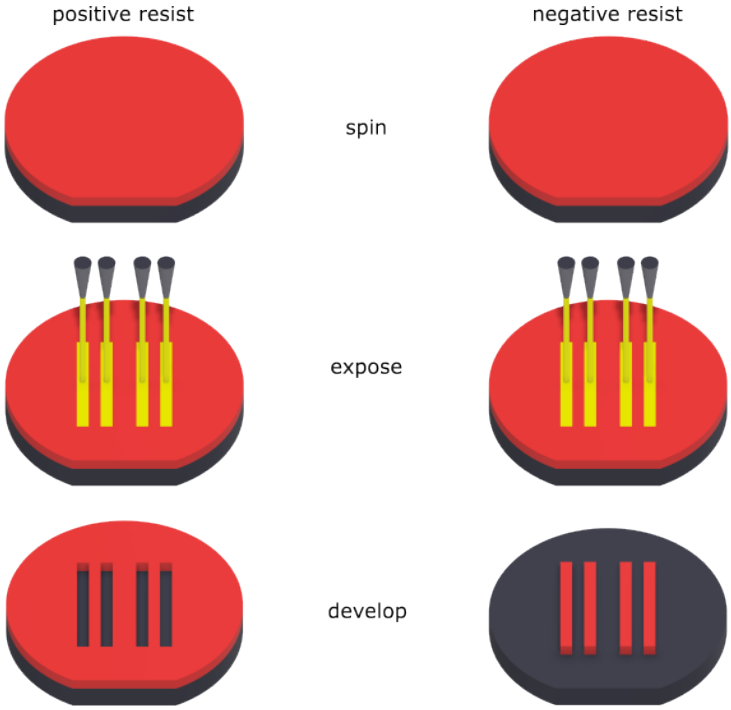

Fig. 2.1 Resist mask formation procedure. On the left a positive resist where the exposed resist will be removed by the developer. On the right a negative resist where the resist hardens from the exposure.

shown in Fig. 2.1.

Positive tone resists consist of long organic chains (e.g. polymers) and undergo chain scissions when exposed. Thus exposed regions become soluble in development chemicals. Negative tone resists are soluble before exposure, they are usually based on free radicals. When exposed, cross linking appears and the resist become insoluble. Usually the type of resist is chosen in a way that exposure time can be minimized. The type of exposure is dependent on the required precision and resolution. Fabrication often includes multiple iterations of the techniques described in this chapter, defining different circuit elements. Markers, made out of niobium or gold and are used for the alignment between the different lithographic layers. Aluminum markers showed lack of contrast in the available e-beam system. In this work, these markers are done in a separate lithography step at the beginning of the sample fabrication.

2.4.1 Optical (Laser) Lithography

Big structures $> 1\,\mu$m can be written with a laser writer. The laser writer offers higher patterning speed at the cost of precision and resolution. A laserwriter from *Microtech* with a 405 nm Gallium Nitride laser diode is used. One can choose between four lenses with different resolution. Substrates are placed on the vacuum chuck of a translation stage. In the y-direction the stage is moved continuously under the fixed laser beam. In the x-direction the laser is deflected at a fixed frequency. By fast blanking of the beam the pattern is generated line by line. The movement speed can be set and is dependent on the lens and complexity of the layout. The applied exposure dose depends on the movement speed and can be adjusted by tuning the gain

of the laser and filters in the optical path of the laser light. The laserwriter offers real time focus adjustment that can correct for an uneven substrate. This is especially important for the high resolution lens, to ensure a sufficient exposure dose.

2.4.2 Electron-Beam Lithography

Electron-beam lithography is the method for fabricating all small ($< 1\,\mu$m) features in the clean room. It is also used for bigger features when higher precision and resolution than possible with the laser writer is required. A detailed description can be found at Ref. [25, 26]. The de Broglie wavelength of an electron is much smaller than that of an optical photon. Thus better resolution can be achieved with electron lithography compared to photo lithography. At *QNZT* a *Raith e-line plus* 30 kV lithography system is used.

Electrons are emitted from the tip of a single crystal tungsten cathode via field emission. In a subsequent stage the electron beam is accelerated to the desired voltage. A set of electromagnetic lenses will focus the beam onto the substrate. Beam diameters of only a few nanometers at the sample can be achieved this way. A beam limiting aperture in the electro optical axis sets the angle under which electrons can enter the focusing system. Thus the aperture sets the beam current and achievable beam spot size. Bigger apertures allow for faster writing at the cost of resolution. A manual aperture alignment is necessary as the apertures are changed mechanically. If not aligned properly with the optical axis, astigmatism and focusing problems can occur. For an optimal exposure the beam shape should be perfectly round. The astigmatism corrector compensates beam imperfections by creating an electrical astigmatism, the intrinsic and artificial astigmatism will cancel each other out.

A deflection system can move the beam in x- and y-direction across the substrate. This is done in a vector style manner where only areas to be exposed are patterned. An electromagnetic beam blanker is used to block the beam when necessary. Besides the beam diameter, the resolution is dictated by the beam step size, that sets the size of a pattern pixel. At each pixel position the beam is held stationary until the desired exposure dose is reached, this time is called the dwell time. The area reachable by the beam is called writefield. Different writefield sizes are realized by changing the zoom factor. The machine corrects for astigmatism of the beam due to the deflection but this is only sufficient to a certain degree. Bigger write fields also result in an increased minimal step size as the DAC that controls the deflection system has a resolution of 2^{16}. The machine fills the layout with an integer number of step sizes, fractions of step sizes will be neglected. The patterning path can be set to meander or line mode. The meander mode is faster but for critical structures I recommend the line mode in combination with dynamical compensation.

The sample is clamped to the chuck of a laser interferometric stage. If the layout exceeds the size of a writefield the stage is moved and the next writefield can be exposed. Automatic alignments after a certain time, by taking an image of markers on the sample for example, help to avoid drifts between stage and write fields. The focusing of the beam onto the substrate has to be adjusted manually at the beginning of an exposure by changing the working distance. Once the focus is set at a single position on the sample the machine offers a laser height sensing tool to readjust it automatically when the stage is moved. I recommend to use this tool for small critical structures spread over larger areas. Due to backside contamination, the wafer will most likely not be perfectly flat on the substrate holder moving the sample out of focus when scanning

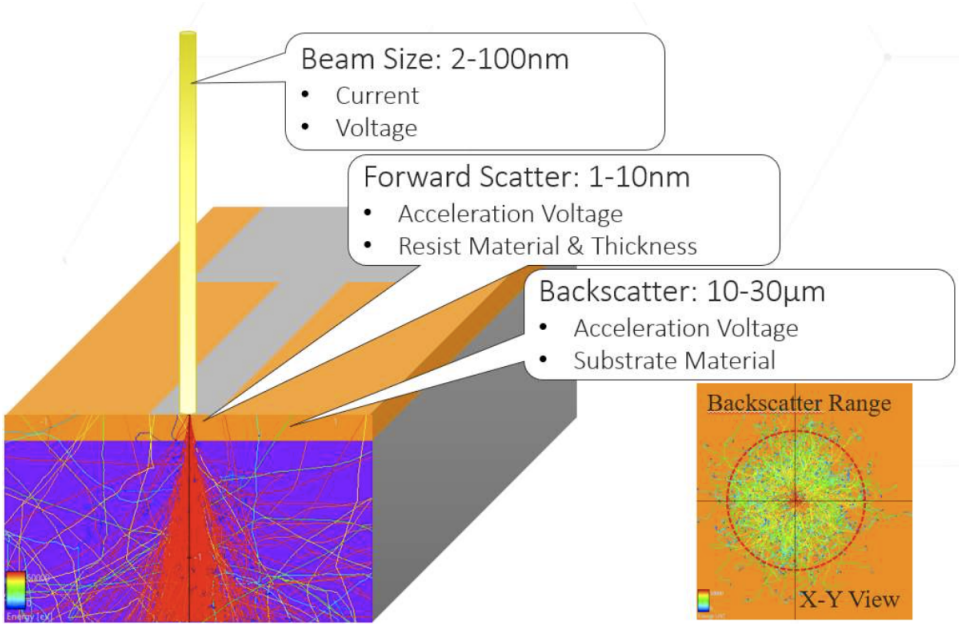

Fig. 2.2 Scattering in electron beam lithography. Broadening of the resist mask due to scattering events is limiting the achievable resolution, this is known as the proximity effect. This figure is used with the kind allowance from *GenISys GmbH* [27].

across the wafer.

The final quality of the electron beam is set by the grade of the electron optics and the focusing ability. Unfortunately, the scattering of the electrons with the resist or substrate, limits the resolution of the final pattern [25, 26]. This scattering can be split into several cases that will be explained below. A schematic is shown in Fig. 2.2.

Forward scattering is the result of low energy elastic collisions of electrons with the resist. Each collision will deflect the electrons by a small amount. The forward scattering leads to a statistically broadening of the beam. The effect increases with resist film thickness. Electrons of higher kinetic energy undergo less forward scattering events and thus the beam broadens less.

Inelastic collisions of electrons and resist are the ones that mainly contribute to the scission/ cross-linking of the resist. As the inelastic events lead to ionization, secondary electrons are generated. Secondary electrons are of lower energy but can still contribute to the loss of resolution.

Most electrons will not be absorbed by the resist and penetrate deep into the substrate. Back scattering results from the reflection of such electrons reemerging into the resist. As the scattering angles can be large this leads to unwanted exposure sometimes far away from the incident beam.

If there is no dissipation channel for the electrons absorbed by the substrate, charging effects will occur. This charge will cause an electric field that can lead to defocusing of the beam.

The effect is especially pronounced for insulating substrates such as sapphire. When using an insulating substrate a conductive layer below or above the resist is thus needed.

To reduce forward scattering, higher acceleration voltages are used so that finer patterns can be drawn. A thinner resist will help for small structures as the aspect ratio between height and width of the mask is less demanding. The back scattering becomes deeper but wider with increasing acceleration voltage. In general high acceleration voltages are known to achieve higher resolution patterns [25]. The best EBL systems available offer acceleration voltages of 100 kV and more.

If pattering areas of different size or dose requirements are placed close together the scattering events lead to increased effective exposure doses in neighboring areas. This will broaden the effective area of exposure, a phenomenon known as the proximity effect. The proximity effect is the main limiting factor of electron beam lithography. As both forward and backward scattering distributions are of Gaussian shape the resulting energy distributions can be calculated. Proximity effect correction (PEC) algorithms can help to reduce the proximity effect by adapting the exposure doses to these energy distributions. PEC software fractures the layout into small trapezoids and calculates an adapted exposure dose from the effective dose.

2.5 Development

Development is the selective dissolution of resist into a relief image that will serve as a fabrication mask [28]. Typically immersion development is performed where the substrate is placed in a beaker of liquid developer. The developer surrounds the smaller resist fragments first, detaching them from the resist matrix before they finally diffuse. With increasing fragment size the bonding to the matrix becomes stronger and fragments less mobile [26]. Thus primarily the small scission fragments (positive resist) or non-cross-linked molecules (negative resist) are dissolved. The development process has to be actively stopped. Special stopper chemicals are available from the manufacturers but for most resists water or pure IPA are sufficient. I prefer IPA myself as it is easier to remove with the N_2 gun due to its higher volatility. This is especially important if one has two resist layers with different developing chemicals as leftover water can block the development of the bottom resist layer.

How far the dissolution extends into the resist matrix depends on time and temperature. A lower temperature leads to a slower development process. In the case of polymers cold development freezes out the dissolution of all but the very smallest fragments. This results in very high resolution of the obtained mask as most electrons scattered during exposure cause insufficient exposure dose to reach the dissolution threshold [26]. Development is strongly correlated with the exposure dose. High exposure dose and short development can result in similar structures than low exposure doses followed by an aggressive development [26]. Considering the error one can make transferring the chip form the developer to the stopper a slower but longer development process has a lower relative error.

It is good practise to agitate the chemicals during development to circumvent saturation of the solvent by diffused resist. The overall resist film thickness can change from the development process. This has to be considered for shadow evaporation processes where the feature size can depend on the film thickness. In case of optical resists developers are often TMAH based. One

has to be careful as TMAH is known to etch Aluminum. If Aluminum etching should be avoided an alkaline developer should be chosen. Only after development optical resist can be exposed to any other than yellow light.

A hard bake after development can help to cross-link the resist and make it more resistant to etching processes. At increased temperatures a re-flow of the resist can occur. This can be used to reduce etch roughness but can also lead to size variations from the exposed image.

2.6 Circuit Formation

At this step the resist mask fabrication is done and one can define the desired structures on the substrate. There are two main techniques to achieve this. Firstly additive deposition of materials via evaporation or sputtering and secondly subtractive etching processes. In both cases the mask will shield parts of the substrate resulting in the circuit formation. In case of evaporation, excess material deposited onto the resist will later on be removed together with the resist by lift-off. Only material attached to the substrate or previously defined circuit layers will remain. In case of subtractive processes, material is added on the substrate before the resist coating. The removal of material is then only possible where the mask is not shielding it.

2.6.1 Evaporation

Thermal evaporation is the additive technique used to deposit all metallic thin films during this thesis. Material is evaporated from a crucible using a high energy electron beam [28]. Evaporated atoms leave the crucible on a straight line path until they collide with other gas molecules or the substrate. To ensure a sufficient mean free path, evaporation has to take place in high vacuum chambers ($< 10^{-6}$ mbar). Vacuum also guarantees the suppression of impurities in the thin film and material source originating from e.g. oxidation. When an evaporated atom hits the much colder substrate it will condensate and stick to the surface. The evaporation rate strongly depends on the boiling point of the material and can be tuned by the available range of electron beam power. The evaporated film thickness can be measured using a quartz crystal oscillator. A PID controller ensures stable deposition rates. The substrate is blanked by a shutter until the evaporation rate is stable. This shutter is placed back in front of the substrate once the desired film thickness is reached. The uniformity and grain size of the metallic thin films depend strongly on the temperature of the substrate and the evaporation rate [29, 30]. Lower deposition rates are suspected to form smaller grains as the condensating atoms have more time to thermalize [15].

The main evaporation system at *QNZT* is a *Plassys MEB550S* that can evaporate Titanium, Niobium and Aluminum. The sample holder can be rotated to arbitrary tilt and planetary positions. As the evaporation is a directional process, material can be deposited onto the substrate under a specific angle. This enables the possibility of shadowing certain areas of the substrate by a resist mask. Using different angles, area selective depositions can be obtained within one vacuum cycle.

When operating the system it is pumped for at least 1 hour to reach the desirable vacuum. The evacuation of the load lock from ambient air is challenging as water molecules are resilient to pumping. When sufficiently low pressures are reached a Titanium gettering step helps to further

improve the vacuum.

The *Plassys* system offers the possibility of oxidation within the vacuum chamber. Thus well controlled oxide layers can be grown on top of the thin films. This is even possible between different depositions as pure oxygen at mbar pressures can be evacuated from the chamber within minutes.

2.6.2 Etching

Dry etching uses the plasma phase of ionized gases to achieve mechanical, chemical or a combined etching [28]. Argon ion Ar^+ beam etching is a mechanical dry etching process where the kinetic energy of the ions is used to mill the target. The ion plasma is accelerated by a potential difference and directed onto the substrate as a focused beam. As it is a purely mechanical etching process a wide range of materials can be etched. The etching rate strongly depends on the acceleration voltage and the plasma conditions. As it is a purely mechanical process with predominant direction it can be done selectively by tilting the substrate.

A mild etching of the resist mask before further additive or subtractive processes is called descum. This is known to remove unwanted resist leftovers from the development step leaving a cleaner substrate and removing blockages of small high-aspect-ratio trenches. Descum is performed by oxygen reactive ion etching. The O_2 molecules are split into two separate O atoms that are highly reactive. The oxygen atoms react with the organic resist residues converting them into a gaseous product that can be pumped away. During descum a small fraction of the resist mask will also be removed but this effect is negligible with proper calibration.

An O_2 descum can be done in the *Sentech ICP* plasma etching system. This is done before wet etching or further etching with the *Sentech* system. In the *Plassys* evaporation system an ion beam gun is installed. Descum is performed using a mixture of argon and oxygen to circumvent oxidation of the ion gun electrodes. Pure Ar^+ etching can be performed to remove oxide layers from metals ensuring proper galvanic connection between different layers.

Wet etching is the purely chemical removal of material by liquid etchants. For the fabrication during this thesis *Transene Aluminum Etchant Type A* was used. It is a mixture of phosphoric-, nitric-, acetic-acid and balanced DI water. Transene is specifically made for integrated circuit devices on silicon wafers and provides an isotropic etch of the aluminum structures. It does not attack common photoresist. The etch rate of the *Transene Type A* is $3\,\mathrm{nm\,s^{-1}}$ at 25 °C. The etching process can be stopped rinsing the sample with DI-water.

2.7 Resist Stripping

The last step of fabrication is the stripping of the resist mask without damaging the fabricated structures underneath. This is done by wet or dry etching of the organic resist mask. In case of a subtractive process this can be done in a fast and effective way.

For additive processes one speaks of a lift-off as the excess material sticking to the mask is removed in the same step. The challenge is to leave no residues from the excess material while keeping the circuit structure intact. For liftoff processes an undercut profile in the resist mask

is recommended. This undercut prevents circuit material on the substrate to also attach to the material at the resist wall. A schematic of an undercut profile can be seen in Fig. 3.4(g). Material attached to both substrate and excess material could be stripped of the substrate during lift off. Small undercuts can be achieved using a stack of a high sensitivity bottom and low sensitivity top resists.

Liftoff is usually performed in liquid solvents as the excess material can shield the resist from being removed. For most e-beam and optical resists acetone or NMP can be used, some resists e.g. *CSAR* require special remover chemicals. Heating the remover results in better solving properties. I usually place the substrate in heated remover for several hours to make the lift-off as gentle as possible. Sonication can help to improve the process. A proper cleaning of the substrate is required after liftoff to circumvent any kind of residues.

2.8 Dicing

As people tend to fabricate multiple devices on one wafer substrate dicing of the sample is often required. Silicon can be cleaved by cutting it with a diamond tip and braking it with a little bit of pressure afterwards. One has to be careful as the silicon tends to brake along its crystal axis. The two crystal axis are usually in parallel and orthogonal to the wafer flat. Cleaving doesn't work for sapphire wafers as there are no preferred axis.

The second option available is to cut the chips with a laser dicer from *Coherent*. A high power pulsed laser evaporates the substrate material which is pushed to the backside by a nitrogen nozzle. The backside has to be free so that an exhaust system can remove the excess material. The laser is more accurate but requires the gluing of silicon substrates to a copper stencil for support. The nitrogen pressure would otherwise break the free resting wafer. These copper stencils are design specificly and can be fabricated with the laser dicer from copper sheets. Using the stencils two cutting steps are required for closed shapes as the stencil has to support itself. Sapphire on the other side can be diced without extra support, only leaving small $< 200\,\mu$m bridges. These bridges can later be broken using a scalpel. Dicing can be done with resist on the chip but it seems that the resist is changed by the dicing procedure. It is thus not good practise to laser dice a wafer with a resist mask that has to be used for deposition or etching after the dicing. What is usually done, is to cover the chip with a protective layer of resist, that will be removed afterwards. This has shown to result in less residues from substrate dust.

CHAPTER 3

Josephson Junctions

Below, the underlying physics of Josephson junctions is discussed. Then, different fabrication techniques will be introduced. The chapter then continues to discuss the fabrication of junction test devices made for this thesis including a detailed fabrication recipe for the Manhattan style junctions. Optimization of the fabrication processes will also be discussed briefly.

3.1 Theory

3.1.1 Superconductivity

Superconductivity is a macroscopic quantum phenomenon in which certain materials show frictionless flow of electrical current when cooled below a critical temperature T_c. This vanishing of all electrical resistance was first observed in mercury by *Heike Kamerlingh Onnes* in 1911 [31]. Warming up a superconductor, a phase transition occurs at T_c and the resistance returns to a finite value called the normal state resistance R_N. R_N afterwards increases with temperature. In 1933 *Meissner* and *Ochsenfeld* discovered superdiamagnetism in superconductors [32]. The phenomenon was named Meissner Ochsenfeld effect and explains the expulsion of all magnetic field inside a superconductor.

The most accurate theory of superconductivity to date is BCS theory [33]. It gives a microscopic explanation of the macroscopic effect. In BCS theory two electrons form a so called Cooper pair. The pairing is caused by an attractive force between electrons, mediated by the exchange of lattice phonons. In contradiction to electrons, Cooper pairs have the properties of a Boson. The bosonic cooper pairs condensate into a new macroscopic ground state. The energy of the new ground state is lower then the Fermi energy of single electrons. The energy difference between the new ground state and the Fermi energy is called the superconducting gap Δ. The macroscopic ground state allows to describe the ensemble of all cooper pairs in a bulk of superconducting material with a macroscopic Bose-Einstein wave function $\Psi = \sqrt{\rho}\, e^{i\phi}$. Here ρ is the superconducting charge density and ϕ is the superconducting phase of the condensate

and e is Euler's number. As the condensate no longer interacts with the lattice or defects in the material the frictionless flow of charge can be explained. The measurement of the superconducting magnetic flux quantum $\Phi_0 = \mathrm{h}/(2\mathrm{e})$ validates the assumption of Cooper pairs with charge $-2\mathrm{e}$ [34, 35].

The dissipationless flow of electrical energy combined with the macroscopic ground state makes superconductors a perfect candidate for building quantum circuits. Common materials used for superconducting circuits include aluminum (Al), niobium (Nb) and tantalum (Ta) [10].

3.1.2 The Josephson Effect

The Josephson effect occurs when two superconductors are coupled by a weak link. It was first predicted by *Brian Josephson* in 1962 during his PhD thesis [1]. For a single electron to tunnel across such a weak link one can observe a probability of approximately 10^{-4}. Prior to Josephson's work it was believed that for a Cooper pair to tunnel across the thin insulating barrier the probability would be the square of the probability for a single electron $(10^{-4})^2$ [3]. Josephson then claimed that the probability of a Cooper pair tunneling is the same as for a single electron as the Cooper pair tunneling has to be seen as one coherent process. *Josephson* was proven right shortly thereafter [2]. One can explain the coherent tunneling process by a coupling of the macroscopic wave functions of the two superconductors. The current introduced by the Cooper pair tunneling is called supercurrent due to its superconducting nature. For supercurrents larger than the critical current I_c of the junction, Cooper pairs split and superconductivity breaks. The critical current is strongly dependent on the weak link and the material of the superconductors.

For the use in superconducting quantum bits the weak link is often chosen to be an insulating barrier. In Fig. 3.1 a schematic of a superconductor-insulator-superconductor (SIS) Josephson junction is drawn. A SIS Josephson junction consists of two superconducting electrodes (grey) separated by an insulating layer (green) in the area where the electrodes overlap. As the material of the superconductors is usually fixed, the properties of the Josephson junction depend on the area and thickness of the insulating barrier.

The Josephson effect in a SIS junction can be fully described by two equations. The first Josephson equation

$$I(\phi) = I_c \sin\phi, \tag{3.1}$$

states that the super current I across a junction varies sinusoidal with the phase difference $\phi = \phi_2 - \phi_1$ of the two superconducting electrodes. The second Josephson equation

$$\frac{d\phi(t)}{dt} = \frac{2\mathrm{e}}{\hbar} V, \tag{3.2}$$

relates the change in phase difference to a voltage V across a junction. This manifests itself in an oscillating super current if a DC voltage is applied across a junction. Substituting the derivative of Eq. 3.1 into Eq. 3.2 gives

$$V(t,\phi) = \frac{\hbar}{2\mathrm{e}} \frac{1}{I_c \cos(\phi(t))} \frac{dI}{dt}. \tag{3.3}$$

This formula has a voltage-current relation like an inductance $V(t) = L\frac{dI}{dt}$. Thus a Josephson junction can be seen as an nonlinear inductance with sinusoidal dependency on the phase difference. Additionally a Josephson Junction has a capacitance C_J do to its geometry having to

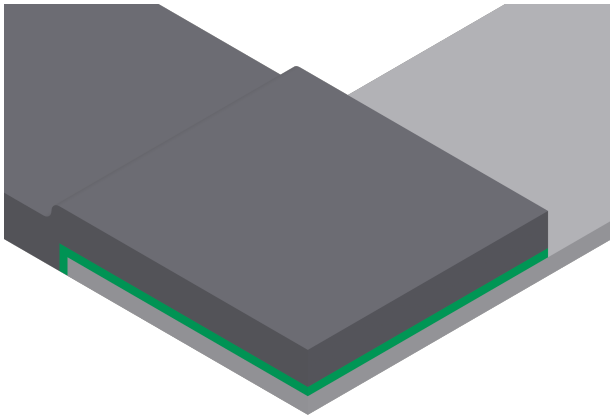

Fig. 3.1 Schematic of a Josephson Junction. In green the insulating tunnel barrier between the two superconducting electrodes. The width of the electrodes determines the junction area. The junction area and the thickness of the barrier influence the physical properties of the junction.

parallel metallic plates separate by a dielectric (see Fig. 3.1). This capacity has no link to the Josephson effect .

The Inductive energy stored in a Josephson junction can be obtained using Eq. 3.1 and Eq. 3.2

$$E_{L_J} = \int_0^t IV dt = -I_c \frac{\hbar}{2\mathrm{e}} \cos(\phi) = -E_J \cos(\phi), \tag{3.4}$$

the maximum energy E_J is called the Josephson energy. It depends only on the critical current.

Finally the critical current I_c

$$I_c R_N = \frac{\pi}{2\mathrm{e}} \Delta(T) \tanh\left(\frac{\Delta(T)}{2\mathrm{k_B}T}\right), \tag{3.5}$$

can be calculated from the *Ambegaokar Baratoff* formula [17]. The normal state resistance R_N of the junction depends on the tunnel barrier properties, the superconducting gap Δ, on the material and thickness of the electrodes. For very low temperatures $\Delta(T) \gg 2\mathrm{k_B}T$ the tanh part can be approximated to 1, leaving the Formula

$$I_c = \frac{\pi}{2\mathrm{e}} \frac{\Delta}{R_N}. \tag{3.6}$$

One can see that a Josephson junction can be characterized by measuring the normal state resistance of the Junction. This is one of the important takeaways for this thesis. It should be noted that the normal state resistance R_N is defined just above the critical temperature of the superconducting material. Measuring at room temperature the resistance of the insulating barrier decreases. This has no relevance for the relative variation of the resistance but one has to account for this when calculating I_C. For this thesis a factor will be included into an effective superconducting gap Δ_{eff} and the room temperature resistance will be referred to as normal state resistance R_N.

The normal state resistance R_N can be divided into two contributions

$$R_N = \frac{R_J}{A} = \frac{R_J}{d^2}, \tag{3.7}$$

the unit-area resistance R_J and the area of the junction A. Assuming squared junctions the area can be expressed by a junction width $A = d^2$. This means that one can tune the junctions critical current and all related properties to a desired value by changing junction area or unit-area resistance. It should be clear that these are also the channels that will introduce variations to the junctions.

3.2 Junction Fabrication Techniques

Since the theoretical background of Josephson junctions should be clear now, the next step is to explain how they can be fabricated. There are several techniques that all have their pro and cons. This thesis will be restricted to the fabrication of Al/AlOx/Al junctions as they are the most common ones for qubits. Aluminium has the advantage of a well controllable oxide formation with the oxides being insulators. To achieve good control over the oxide formation the junctions are fabricated within one vacuum cycle. Forming a Josephson junction this way could be done by just two flat Al depositions with a oxidation step in between. The difficult part of fabricating usable Josephson junctions is to access and connect each electrode of the junction to the circuit without shorting the junction or forming unwanted parasitic junctions. This can be achieved by making use of the directional evaporation processes in combination with geometrical considerations for a lift-off process resist mask design. The area of the junction is then set by the size and overlap of the electrodes. The unit-area resistance will be mainly set by the time and pressure of the oxidation.

3.2.1 Dolan Bridge

The Dolan bridge technique was proposed by *G. Dolan* in 1977 [36, 37]. The resist mask used to fabricate these junctions makes use of a suspended bridge structure. A schematic for the Dolan bridge technique can be seen in Fig. 3.2. The bridge is achieved by using a high sensitivity bottom resist and a low sensitivity top resist Fig. 3.2(a). For the deposition of the first junction electrode (Fig. 3.2(b)) the sample is tilted by an angle $\theta_1 = 24°$ along the bridge axis. This bottom electrode is shown in blue, it is disconnected where the substrate was shadowed by the bridge. After the first electrode is evaporated the sample is oxidized to form the insulating tunnel barrier. The sample is then tilted to an angle $\theta_2 = -24°$ to form the second electrode, shown in red.

This way a Josephson junction is formed in the area underneath the bridge where both depositions overlap. A SEM image of a Dolan bridge junction can be seen in the inset of Fig. 3.2(e). The areas, where just one evaporation step was deposited directly onto the substrate, can be used to connect the junction to the circuit. The deposition angles θ can be chosen differently and together with the bridge design and the resist height they will set the junction area. As both electrodes for Dolan bridge junctions consist of two parts there is additional stray junctions formed during the process (Fig. 3.2(d)), leading to dielectric losses. In Ref. [38] an in-situ bandaging process has been developed to shorten these stray junctions, leading to improved coherence times, without adding any additional fabrication steps (Fig. 3.2(d)). The most significant disadvantage of Dolan type junctions is the direct dependence of the junction area on the

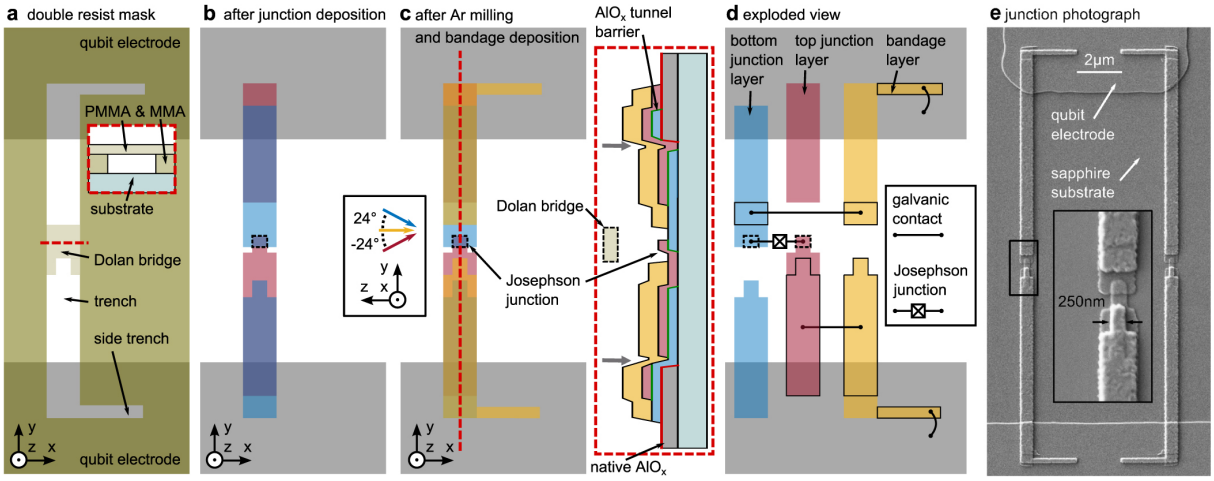

Fig. 3.2 Fabrication scheme for Dolan Bridge junctions. Shadow evaporation from two angles using a resist bridge froms a junction. Figure taken from [38].

exact resist heights and evaporation angle leading to increased variance in junction resistance. Descum processes are complicated by the bridge covering the junction area.

3.2.2 Bridge Free

The Bridge free technique overcomes the need of a suspended bridge by making use of symmetric and asymmetric undercuts [14]. Such undercuts can be formed by using different lithography doses in combination with a high sensitivity bottom resist and a low sensitivity top resist. The resist mask for a bridge free junction consists of two wires with asymmetric undercuts (Fig. 3.3(c & e)). In between the two wires there is a wider electrode area with a symmetric undercut (Fig. 3.3(c)).

The first deposition is done under an angle θ_1 forming the upper wire and bottom junction electrode, green in Fig. 3.3. The area of the lower wire is protected by the resist undercut due to the deposition angle. All material getting into the opening for the lower wire will be deposited onto the resist wall and thus removed during the lift off. After the first deposition the insulating oxide layer is formed. A second evaporation under angle θ_2 forms the lower wire and top junction electrode, red in Fig. 3.3. A SEM image of a bridge free junction can be seen in Fig. 3.3(a). In principle there is no undercut needed for the junction area but liftoff processes are known to be more reliable with undercuts, as a physical separation between metal-on-substrate and metal-to-be-lifted-off is achieved.

An advantage compared to the Dolan bridge junctions is the better access to the junction area for descum procedures and a more robust resist mask allowing for a greater accessible range of junction size. Similar to the Dolan bridge junctions the direct dependence on resist height and deposition angle on the junction area is a disadvantage. Additionally the asymmetric undercuts add complexity to the mask fabrication. Bridge free junctions were the standard in the *Innsbruck Circuits* group at the start of this master thesis.

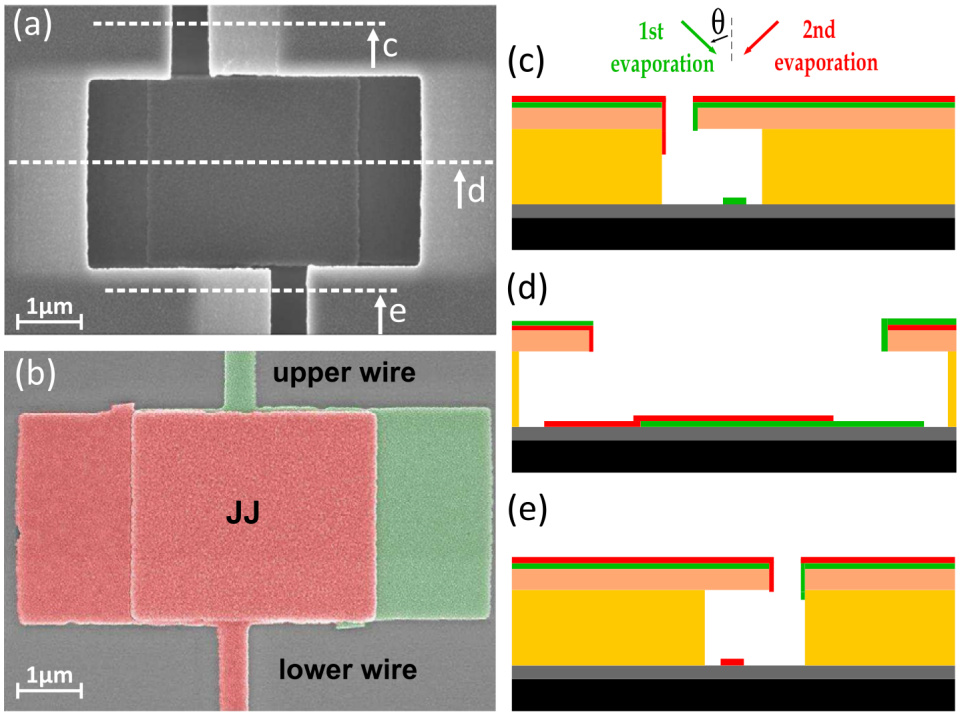

Fig. 3.3 Fabrication scheme for Bridge free junctions. Asymmetric undercuts allow for the selective connection to the junction electrodes. Figure taken from [14].

3.2.3 Manhattan Style

Manhattan Style also called cross type Josephson junctions were first proposed by *Potts et al.* [39]. The resist mask for a Manhattan junction consists of two trenches with a respective angle of 90° forming a cross shaped pattern, as can be seen in Fig. 3.4(a-b). The width of both trenches d is usually chosen to be the same. The length of the trenches l is much greater than their width d. The resist mask is fabricated with a thickness s. In addition to the tilt angle θ a planetary angle φ is used for the deposition of the electrodes.

The deposition of the first electrode is performed under angles $\theta_1 = -45°$ and $\varphi_1 = 45°$ as shown in Fig. 3.4(d-g). In Fig. 3.4(d) the resist mask is shown from the evaporation direction for θ_1, φ_1. For one of the trenches the substrate will be exposed to the evaporated metal, forming the bottom electrode of width d. The only part of the bottom electrode that will be partially shadowed due to the resist height is resulting in shortened electrode length $l - s \cdot \tan\theta_1$. The second trench will be fully shadowed by the resist mask if $s > d \cdot \tan\theta_1$.

After deposition of the bottom electrode the oxidation for the tunneling barrier is performed, as shown in Fig. 3.4(h-i). Deposition of the top electrode is performed under angles $\theta_2 = -45°$ and $\varphi_1 = -45°$. Here the same geometrical considerations as for the bottom electrode apply. The Josephson junction will be formed where both electrodes overlap as indicated in pink in Fig. 3.4(l). This area is set by the width of the electrodes $A = d^2$. As d is the width of the trench there is no geometric dependence of the junction area on the resist height. The junction area is also independent of the tilt angle θ. The influence of the planetary angle φ has a cosine dependence and can therefore also be neglected in terms of small-angle approximations.

An undercut is not necessary for a Manhattan style junctions but it will simplify the lift off procedure and give better junction yield. In Fig. 3.4(g) a trench with an undercut profile is shown. The electrode width d is set by the mask forming top resist, the undercut will have no influence on the width of the electrodes. However, one has to consider the undercut width u for the shadowing of the trenches ensuring $s > (d+u)\tan\theta$ is still valid.
As the bottom electrode shadows the top electrode at the side further away from the evaporation source the circuit has to be connected from the electrode side closer to the evaporation source to avoid an open circuit. On the further away side the electrodes are designed longer than required for the junction formation. This is done, to keep liftoff artifacts, that can occur at this end of the electrodes, far away from the junction area.

Due to the relatively easy mask fabrication, Manhattan junctions allow for fabrication of very small junctions. Junction of micrometer size on the other hand become complicated as resist heights have to increase drastically. If multiple junction sizes are required within one fabrication run a trade of between smallest and biggest possible size has to be done as the aspect ratio between required resist height and small trench width becomes a challenge for lithography.

3.3 Experimental Requirements

The aim of this thesis is to not only characterize the reproducibility of junctions but also study the influence of different junction parameters such as junction area and oxidation parameters on the normal state resistance. To assure meaningful statistics the amount of junction has to be of certain size and optimally one can distinguish the sources of spread. Different junction sizes can be realized in the same fabrication run. Different oxidation parameters need separate deposition cycles. On the other hand the fabrication should be as time saving as possible. Combining these requirements leads to fabricating multiple chips of test devices in one run and dicing them into separate chips before the junction deposition. This procedure should also minimize variation in all the fabrication steps previous to the deposition.

It was decided to fabricate 6x6 = 36 chips of size $5\,\mathrm{mm} \times 5\,\mathrm{mm}$ on a 2 inch Si wafer. This was considered a good compromise between chip handling size and throughput. In Fig. 3.5(a) the fabrication layout for a wafer of test devices is shown. A total of 9 different junction sizes was fabricated. The junctions were designed with symmetric electrode widths between $100-300\,\mathrm{nm}$ and a linear spacing of $25\,\mathrm{nm}$. The total amount of junctions on a wafer is limited by the write time of the e-beam lithograph. It was aimed to write all junctions on a chip within an overnight exposure.

The junction electrodes are so small that they cannot be probed directly. This is why in addition to the junctions, probing pads had to be fabricated. At the edges of the chips about $1\,\mathrm{mm}$ had to be reserved for clamping them on the *Plassys* sample holder. This also helps to avoid the influence of edge effects on the resistance measurements. Taking all consideration into account resulted in the chip design shown in Fig. 3.5(b). The chips consists of 29 columns and 7 rows of probing pads. The first and last column of pads are reserved for intentional shorts to calibrate out the offset resistance resulting from electrodes and pads (Fig. 3.7(d)). This leaves space for 21 junctions of each of the 9 sizes. They are placed in alternating order from the smallest to the

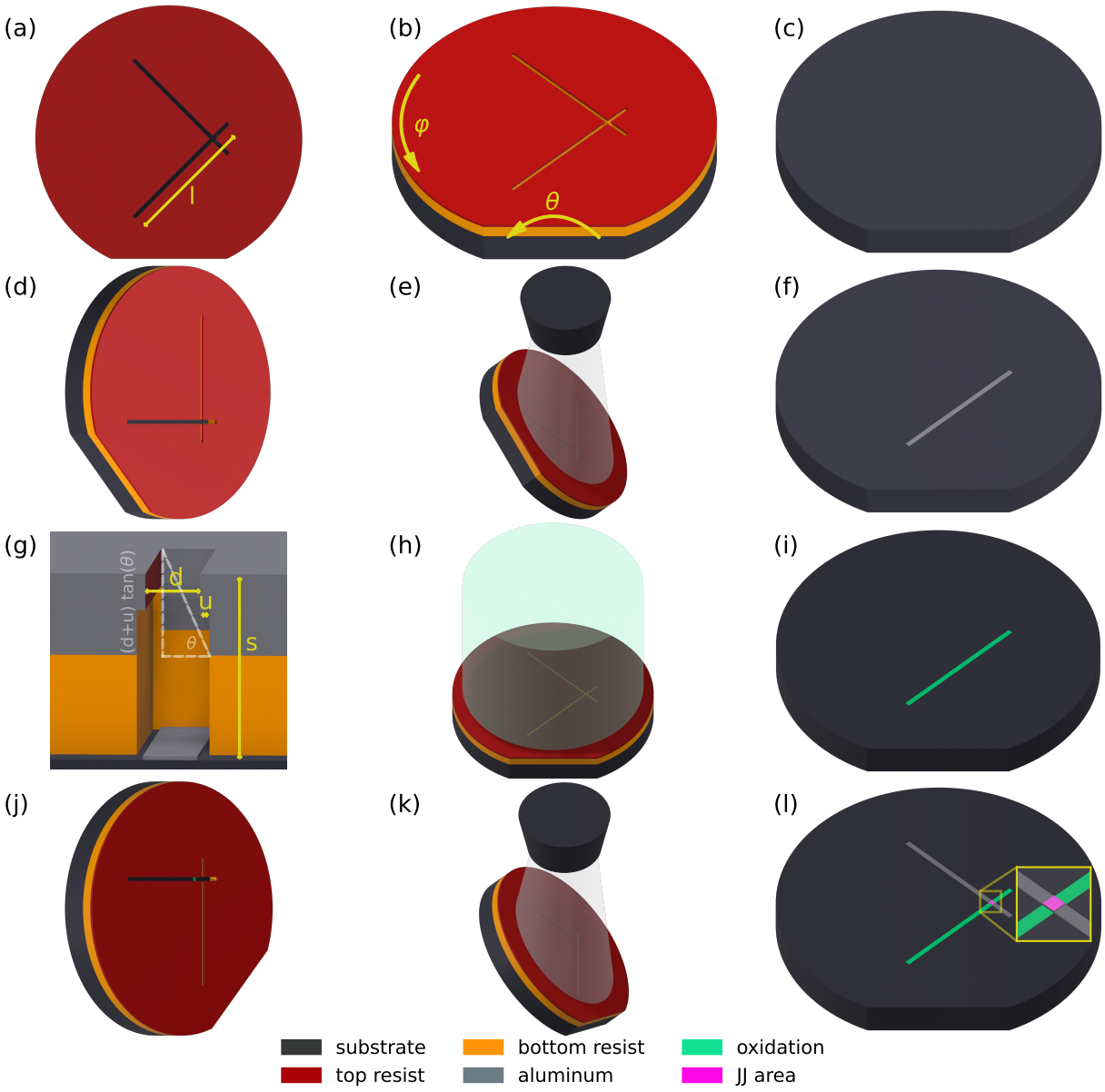

Fig. 3.4 Manhattan style Josephson junction fabrication. (a-c) Before junction evaporation. (d-f) Deposition of the first junction electrode. (h-i) Oxidation for tunnel barrier growth. (j-l) Deposition of second junction electrode. Deposition on the resist is not shown except for (g). (g) Cut into the resist layer showing the undercut and geometrical considerations for shadowing. (a, d, j) View from evaporation direction. (c, f, i, l) Result of evaporation if resist would be stripped after the step.

biggest junction size in each row.

One problem that was encountered is the connection between junctions and pads. The pads are fabricated in a separate step prior to the junctions, using the laser-writer and etching, as this is faster and cannot alter the junctions. Usually Manhattan junctions are bandaged in a separate lithography and deposition step after the junctions are finished. This is necessary as the pad/circuit due to its material height shadows the connection area. The bandage is also needed to ensure superconducting connection of the second electrode and pad, without stray junctions resulting from the oxidation of the junction area. In the case of the devices fabricated during this thesis this would mean an extra lithography step for every chip. This would be a huge effort even when combining bandaging deposition.

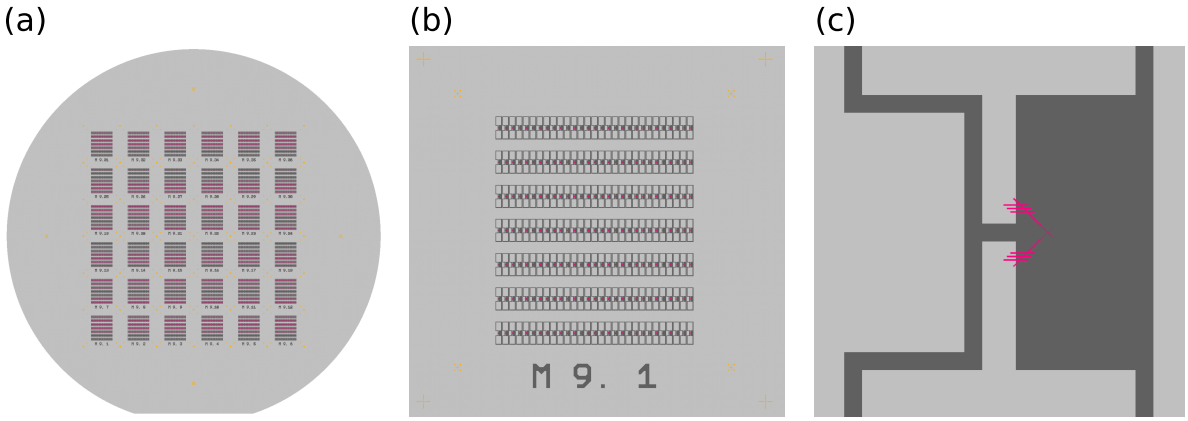

Fig. 3.5 Fabrication layout for the junction characterisation. (a) Each 2 inch wafer has 36 identical chips. (b) The 5 mm × 5 mm chips have 7 rows and 29 columns of probing pad pairs. Each electrode of a junction is connected to one of the probing pads (c). A row starts with a shorted junction of the smallest size and ends with a shorted junction of the biggest size. In between the shorts each row contains 3 of 9 different junction sizes in alternating order. This gives 21 junctions of the same size on each test device.

3.4 PICT Process

To overcome the necessity of a separate bandage Layer the patch-integrated cross-type (PICT) process was adapted to the junction fabrication. PICT was first introduced by *Osman et al.* [16] and enables in-situ bandaging during the junction deposition cycle. This is possible adding a third set of evaporation angles θ_3, φ_3. A schematic of the PICT process is shown in Fig. 3.6. Different to the standard resist mask for a Manhattan junction the PICT mask has additional fringes of width f in a 45° angle to the electrodes. These fringes overlap with the circuit, Fig. 3.6(a-c). With the correct geometrical considerations milling and deposition of these fringes can be done selectively. The first steps of evaporation cycle are the same as for the common Manhattan process.

Fig. 3.6(d-f), the bottom electrode is deposited under angle φ_1, θ_1. To ensure there is no deposition onto the fringes $f < s/(\sqrt{2}\tan(\theta_1))$ has to hold. Same as for the standard Manhattan

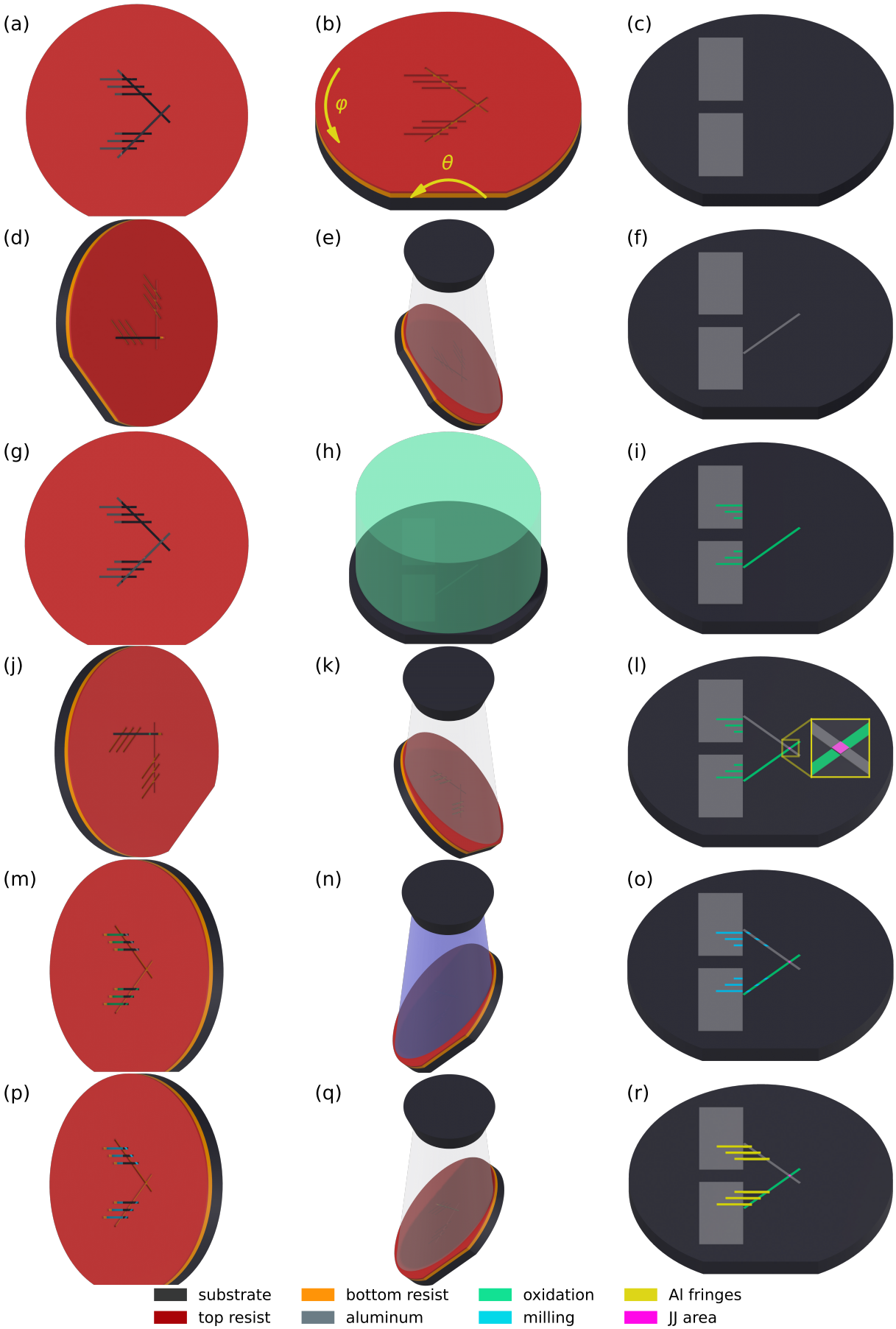

Fig. 3.6 PICT fabrication. (a-c) Before junction evaporation. (d-g) Deposition of the first junction electrode. (h-i) Oxidation for tunnel barrier growth. (j-l) Deposition of second junction electrode. (m-o) Ar ion milling. (p-r) Deposition of fringes.

process $s > d\tan\theta_1$ has to hold to ensure shadowing of the second trench.
Fig. 3.6(g-i), oxidation for tunnel barrier formation is performed afterwards. In addition to the bottom electrode the circuit will be oxidized at the location of the fringes.
Fig. 3.6(g-i), the top electrode is formed under angle φ_2, θ_2, the geometrical considerations are the same as for the bottom electrode. At this point the Manhattan junction itself is formed.
Fig. 3.6(m-o) An argon ion milling at angles θ_3, φ_3 is performed to remove oxides at the location of the fringes. This is necessary to ensure proper galvanic connection between junction and circuit without forming stray junctions. If $s > d\tan(\theta_3)\sqrt{2}\cdot 2$ is valid the junction area will be protected from the milling.
Fig. 3.6(p-r) After milling the fringes can be deposited under the same angles θ_3, φ_3 as the milling was done. The circuit and the junction are now successfully connected and liftoff can be performed.

3.5 Probing Pad fabrication

The fabrication of the junction test devices starts with an empty silicon prime wafer of 2 inch size. The wafer is cleaned by sonication in acetone and IPA and an aluminum layer of 50 nm thickness is deposited. In the next step alignment marks are exposed into a stack of MMA and PMMA using electron beam lithography. 100 nm of Niobium are deposited onto the mask and lifted of afterwards.

Each pad has a size of $80\,\mu\text{m} \times 120\,\mu\text{m}$ and a smaller wire of $10\,\mu\text{m} \times 37.5\,\mu\text{m}$ for the connection to the junction. The pads are defined by wet etching a galvanic separation of $5\,\mu$m width into the aluminium plane. An additional area of the substrate is etched free to facilitate the junction fabrication. This can be seen in Fig. 3.5(c).

The etch mask is exposed in the laserwriter using an *AZ 1505* positive resist layer. After development the sample is put into the *Sentech ICP* for an 20 s oxygen plasma descum. The Aluminum that was deposited before is then wet etched with *Transene aluminum etchant Type A* for 2 min 30 s. According to the manufacturer the etch rate of the Transene Type A is $3\,\text{nm}\,\text{s}^{-1}$ at 25 °C. It is assumed that the oxide layer on top of the aluminum is the reason for the enhanced time necessary to remove all the aluminum. The etching is ceased in H_2O and the wafer is rinsed carefully. The wafer is then placed in acetone at 50°C to remove the resist mask. The removal is finished by sonication in acetone followed by IPA. After drying the sample using the N_2 gun the pad fabrication is finished. In Fig. 3.7(a-b) a SEM image including junctions and pads can be seen. In the next step the junctions can be fabricated.

3.6 Junction Fabrication Recipe

For the Josephson Junctions a resist bi-layer of *MicroChem MMA-EL13* and *AllResist GmbH AR-P 6200.09* (*CSAR*) is used. Previous studies showed that this resist combination is favorable due to the mostly orthogonal development chemistry of *EL13* and *CSAR* resulting in a high fabrication yield [15]. *EL13* serves as the bottom undercut layer due to its high sensitivity. *CSAR* is a high contrast resist that is highly process-stable qualifying it as the masks top layer. First a quantity of 0.3 mL *EL13* is transferred onto the substrate and spin coated immediately thereafter for 100 s at 3000 rpm using an acceleration of $1000\,\text{s}^{-2}$. The substrate is then placed on a hotplate for 3 min at 160 °C to soft bake the resist. *CSAR* (0.2 mL) is spin coated on top

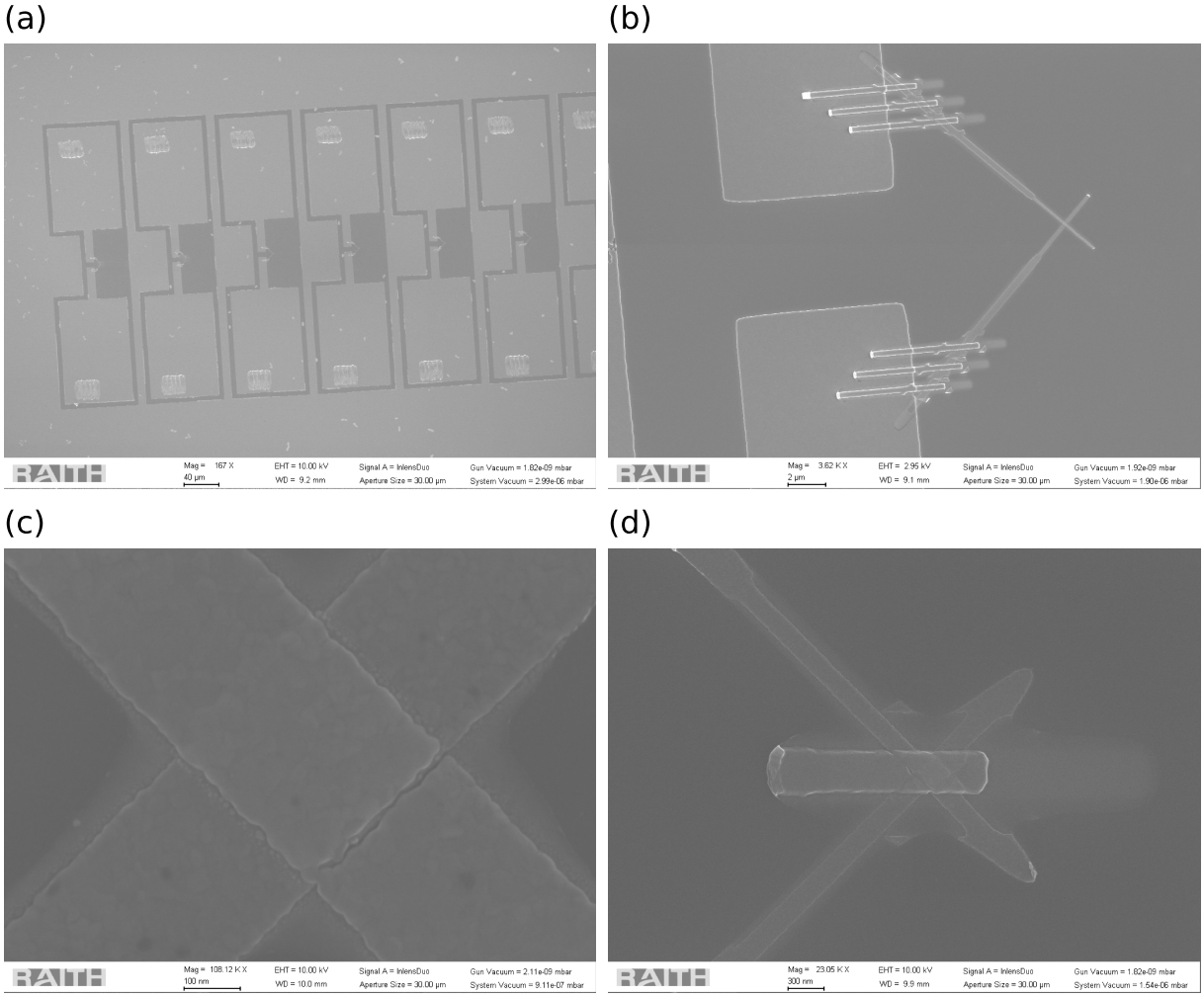

Fig. 3.7 SEM images of a junction test device. (a) Probing pads. In the darker spots the aluminum was etched and the substrate is visible. The white scratches on the pads result from the automatic probe station. (b) Josephson junction connected to the probing pads by fringes. (c) Zoom in on the actual junction area where both electrodes cross. (d) Shorted junction to calibrate the offset of a resistance measurement.

for 100 s at 4000 rpm using an acceleration of $1000\,s^{-2}$ and the wafer is soft baked afterwards for another 3 min at 160 °C. This results in a resist stack of approximately 800 nm *EL13* and 220 nm *CSAR*.

The sample is then loaded to the *e-line* lithography system. A 10 µm aperture and 30 kV acceleration voltage is used for the exposure. The base dose for the given resist stack is set to $130\,\mu C\,cm^{-2}$. A 100 µm write field and 2 nm beam step size is used to write the design features. The exposure is run in line mode in combination with the dynamic compensation option of the machine. The focusing across the wafer is optimized using the optional laser height sensing. Alignment with previously written circuit elements is done via manual three point alignment. During writing an automatic write field alignment using images is done every 15 min for drift compensation.

Proximity effect correction for the junction design was done using *GenISys GmbH BEAMER*. *GenISys* provided us with a PSF File for 970 nm PMMA on Si at 30 kV and a Z-position of 946 nm. According to *GenISys*, the stack of *CSAR* and *EL13* can be approximated by a single layer of PMMA. The total stack height changed during optimization. Additionally an effective short range blur FWHM of 100 nm, an accuracy of 0.5%, a short range separation value of 5 µm, a mid-range activation threshold of 2% and a maximum dose factor of 4 was set in the software.

After the exposure, immersion development is performed. The sample is placed in a small beaker filled with *AllResist GmbH AR 600-546* for 30 s. The sample is slowly moved up and down (using wafer tweezers) during this time, to ensure homogeneous developer concentration. The development is stopped placing the wafer in IPA for a few seconds and rinsing it thoughtfully afterwards before blow drying it with a N_2 gun. The *EL13* layer is then immersion developed by holding the wafer into a bath of 3:1 IPA:H_2O cooled down to 6 °C. Development is stopped using IPA and blow drying the wafer.

The sample is then loaded into the *Plassys* evaporation system. Care has to be taken to correctly align the sample chip to the tilt axis of the sample holder. The system is pumped for at least 1 hour to achieve load lock pressures below 1×10^{-6} mbar. First a descum process using an Ar^+ O^+ plasma (5 sccm each) is performed for 3 min. During this descum the wafer is rotating with 5 rpm. The ion gun discharge is set to 45 V, the beam voltage to 200 V, the accelerator voltage to 50 V and the beam current to 6 mA. After descum, a 2 min Ti gettering is performed to improve the chamber vacuum.

The sample is then rotated to planetary angle $\varphi = \text{load} - 45°$ and tilted to evaporation angle $\theta_P = \text{evap} - 45°$. At this position the first Al junction electrode is deposited at a rate of 0.5 nm/s until a thickness of 20 nm is reached (Fig. 3.6(d-f)). It has to be noted that the tilt angle of the *Plassys* system θ_P is defined 90° rotated compared to Fig. 3.4. In this section it will be referred to the *Plassys* coordinates.

Following the deposition of the first electrode static oxidation is performed to form the tunnel barrier (Fig. 3.6(g-i)). Therefore O_2 is let into the chamber at a rate of 20 sccm, the rate is reduced when getting close to the set oxidation pressure. When the set pressure is reached the inlet valve is closed and the system waits for the set oxidation time. Once the oxidation time is over the chamber is evacuated again by pumping the system.

The sample is then rotated to planetary angle load $+45°$ and tilted to tilt angle evap $-45°$ to evaporate the second junction electrode at a rate of 0.5 nm/s until a thickness of 40 nm is reached (Fig. 3.4(j-l)).

In the next step the in-situ bandage layer is fabricated. The sample is rotated to planetary angle load $+\,0°$ and tilted to angle $\theta_P = \text{etch} + 55°$ ($\theta = 35°$). An Ar^+ ion milling (5 sccm) is performed for 1 min to ensure proper connection between the junction electrodes the circuit and the bandage layer without forming any stray junctions (Fig. 3.6(m-o)). The ion gun discharge is set to 40 V, the beam voltage to 400 V, the accelerator voltage to 80 V and the beam current to22 mA.

Following the milling step, the sample is rotated to $\varphi = \text{load} + 0°$ and tilted to $\theta_P = \text{evap} + 55°$. The bandage Layer is then deposited at a rate of 1 nm/s until a thickness of 120 nm is reached (Fig. 3.6(p-r)).

The process is concluded by a 2 min static O_2 capping at 10 mbar to form a controlled oxide layer on top of the junctions. Following the capping the sample can be unloaded from the *Plassys* evaporation system.

Liftoff is performed placing the sample in a beaker of *AllResist GmbH AR 600-71* at 65 °C for at least 2h. The beaker is then moved to an ultrasonic bath at 50 °C where it is sonicated for 10 min at 130 kHz with 40 % power. The wafer is then transferred into a beaker of IPA. During the transfer the sample is rinsed with IPA from a spray bottle to get rid of as much particles from the lift off as possible. The sample is then sonicated for another 5 min with the same settings as before. After sonication the sample is rinsed with IPA again and is finally blown dry with the N_2 gun. With this step the junction fabrication is done. In Fig. 3.7(b-c) SEM images of a resulting junction are shown.

3.7 Remarks on Fabrication Optimization

The first problem encountered when adopting the PICT process was shorting of the biggest junctions by the evaporation of the fringes. This is shown in Fig. 3.8(b). The first suspicion was that the problem is the width of the undercut. A study of the geometrical considerations later revealed that a factor of 2 was missing for the considerations of the fringe width in the original paper.

The initial idea was to fabricate Manhattan Junctions with electrode widths from $100-300$ nm. It turned out that the reproducible fabrication of such small features is quite demanding. One reason is the required resist height for the PICT process. This makes the aspect ratio for the smallest junctions widths quite challenging due to the relative high resist for the widest junctions. During optimization of the fabrication recipe the widths measured with a SEM were all wider. Thus in the junction layouts the electrodes have reduced widths of $75-275$ nm. This helped to reduce the size but especially for the smallest junction 100 nm width could never be reached this way. The junction width depends, beside the layout, strongly on the exposure dose. Adapting the dose the bigger junction can be tuned to size but for smaller junctions this was not possible. In Fig. 3.8(c) a small junction exposed with low dose is shown, the problem is that

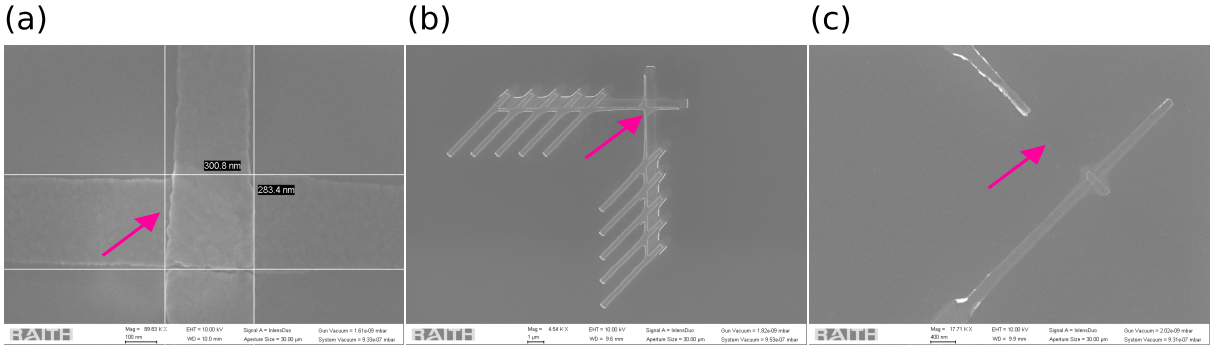

Fig. 3.8 Fabrication problems. (a) Asymmetric junction due to proximity effect. (b) Junction shorted from deposition of bandage fringes. (c) Broken junction due insufficient dose.

part of the layout did not receive enough dose to be sufficiently developed. It was tried to use different resist stacks as well as a single layer PMMA but better results could not be achieved. It is assume that forward scattering in combination with the demanding aspect ratios is the limiting factor. A solution for this would be an e-beam system that offers higher acceleration voltages.

The other problem was that the junctions had shapes that were non rectangular as shown in Fig. 3.8(a). This will lead to partial shadowing of the junction area by the resist mask and thus will reintroduce the junction area dependence on the resist height. This problem was solved by PEC with the *BEAMER* software from *GenISys*. In Fig. 3.9(a) the simulated energy distribution for the PEC is shown. Fig. 3.9(b-c) show the corrected layouts for the smallest and biggest junction. The different colors indicate different dose, where red is highest and blue lowest dose. The parameters for the forward scattering were obtained experimentally doing multiple tests. With the help of the PEC software the size of the junction could also be reduced. Using a $7\,\mu$m aperture a junction width of 100 nm was obtained. The problem was that SEM imaging showed variations of up to 20 nm across a wafer. A drift in current or focus was suspected to cause this. Thus a $10\,\mu$m aperture was used and the laser height sensing for focus correction was implemented to the process. This resulted in the junctions described in the recipe above. The obtainable smallest junction size increased again due to the $10\,\mu$m aperture but results were consistent. As the time for further tests was limited I decided to stay with this fabrication recipe. Reproducibility seemed more important than obtainable size as the normal resistance can be adapted by the oxidation parameters. There is an ongoing discussion in the community if smaller junctions would yield lower TLS and thus dissipation [11].

Further improvement of the recipe could be achieved by optimizing the descum and milling process [15]. Due to time restriction however no further investigation of their influence on the fabrication was performed. There is also ongoing research in how aluminum oxide layer growth can be improved [40–42]. Al film growth conditions seem to have an influence on the homogeneity of the barrier [15, 29]. Other considerations include dynamical oxidation of the barrier [43, 44].

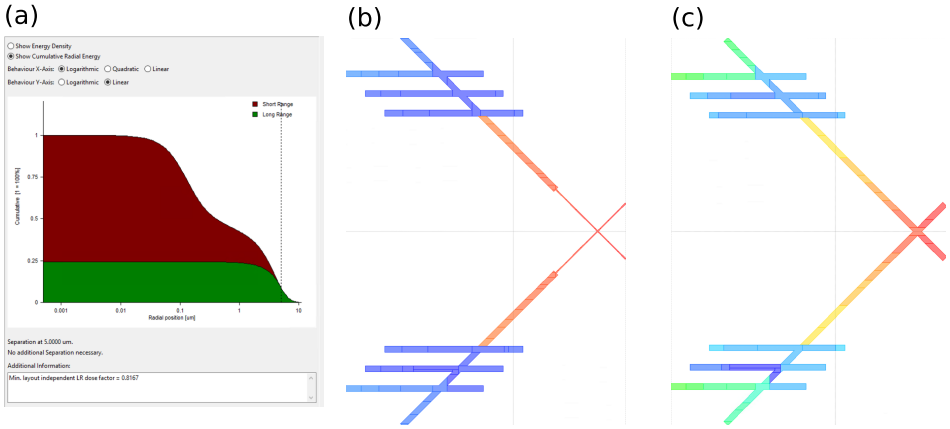

Fig. 3.9 Proximity error correction. (a) Simulated energy distribution. (b-c) Corrected junction layout for smallest (b) and biggest (c) junction. Red color corresponds to the highest dose, blue to the lowest.

3.8 Junction Test Devices

A total of three wafers labelled M9, M10 and M11 was fabricated with the final junction fabrication recipe and cleaved into separate chips after the development of the mask. Chips were then separately evaporated with one of the four oxidation parameter sets. An exception was made for Chips M10.1 and M10.32 that were evaporated together to gain fast knowledge about the spread in parameters of the new recipe. The 4 oxidation parameter sets were chosen to be $p_{ox} = 0.6\,\mathrm{mbar}$ and $t_{ox} = 10\,\mathrm{min}$, $p_{ox} = 0.8\,\mathrm{mbar}$ and $t_{ox} = 10\,\mathrm{min}$, $p_{ox} = 1.0\,\mathrm{mbar}$ and $t_{ox} = 10\,\mathrm{min}$ and $p_{ox} = 1.0\,\mathrm{mbar}$ and $t_{ox} = 20\,\mathrm{min}$. For each wafer a total of 3 chips per oxidation parameter set was fabricated, except wafer M10 where 5 chips with $p_{ox} = 1.0\,\mathrm{mbar}$ and $t_{ox} = 10\,\mathrm{min}$ were fabricated to determine the spread in parameters of the new recipe. In Fig. 3.10 a map for each wafer is shown with the qualitative position of the chip on the wafer. The colored chips are the ones that were used for this thesis. The different colors correspond to the different oxidation parameters. An effort was made to chose the chips randomly. For wafer M11 the right half could not be used as the alignment between junctions and pads failed due to a drift of the laser writer.

Before evaluation of the room temperature resistance of the test devices, a consistency check of some fabrication parameters is performed. In Fig. 3.11(a-b) the measured resist height for the bottom and top resist layers of all fabricated samples is shown. This is the resist stack used for the junction fabrication. The red line and shaded area indicate the mean resist height and the standard deviation respectively. In general a reproducibility of resist thickness better than 5% is achived at *QNZT*, as indicated by the dashed purple lines. At this level of accuracy it is expected that the variations in resist height do not influence the required lithography dose significantly.

In Fig. 3.11(c) The combined height of the resist stack was measured at five different positions. The center of the wafer showed a slightly increased resist height compared to the rest. This small increase should have little effect on Manhattan junctions but would result in a junction area variation for other fabrication techniques. It can be explained by the higher rotational

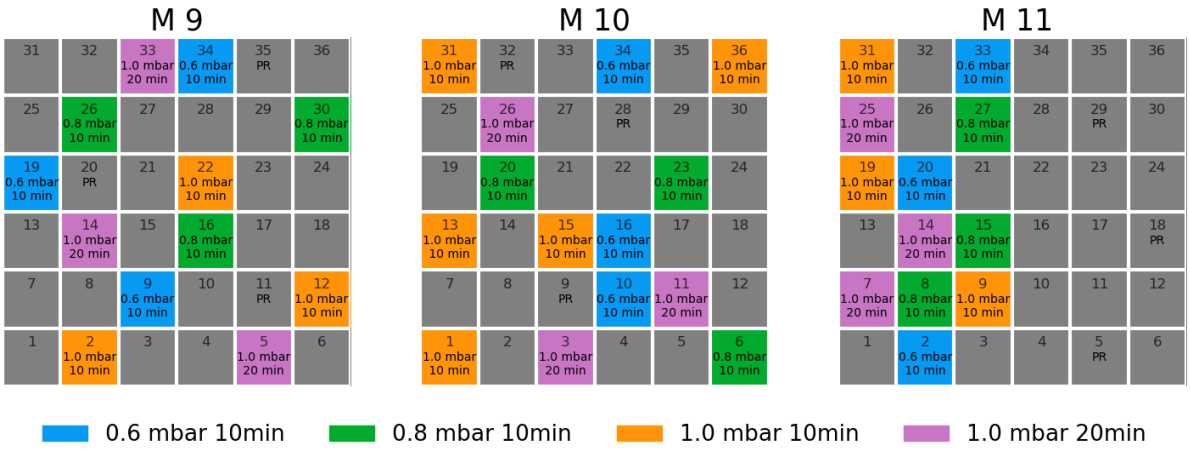

Fig. 3.10 Oxidation parameter map of the chips used for junction statistics. The position of the 5x5 mm chips corresponds to the actual position on the wafer. Colored chips are used for the statistics, colors indicate oxidation parameters. Chips labeled with PR were used to measure the parallel resistance of the substrate.

speeds at the outside of a wafer during spin coating.

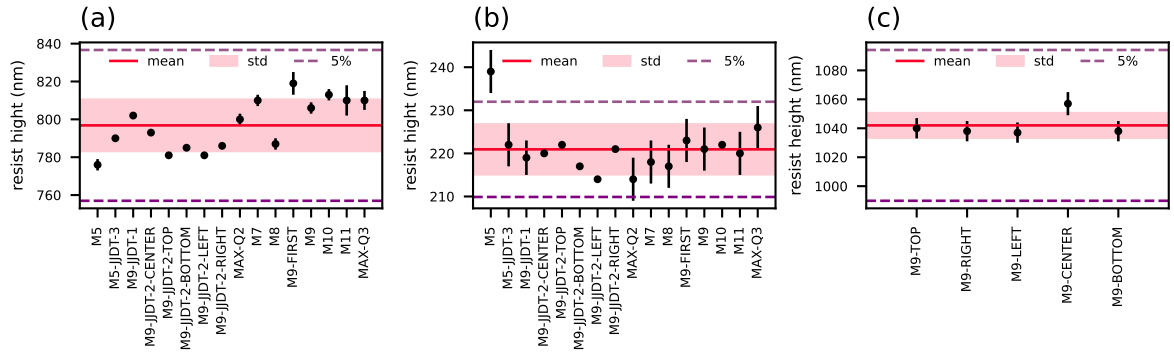

Fig. 3.11 Resist height measured with an ellipsometer for different samples (black markers). The mean and standard deviation across all samples is shown in red. The purple line indicates 5% variation from the mean. (a) The EL 13 bottom resist for the junction fabrication process. (b) The *CSAR* top resist for the junction fabrication process. (c) The height of the combined resist stack for sample M9 at different positions of the wafer.

Another source of error that has to be considered are the stability of the oxidation parameters, time and pressure. Fig. 3.12 shows the rise time till a set oxygen pressure is reached over all junction test devices. The deviations are in the orders of seconds and can be considered negligible in comparison to the oxidation time of multiple minutes.

In Fig. 3.13 the oxygen pressure, as measured by the LP sensor of the *Plassys* is shown over all junction test devices. In red the mean and standard deviation is shown. The dashed lines indicate the target pressures that were set in the software. The deviation between target and

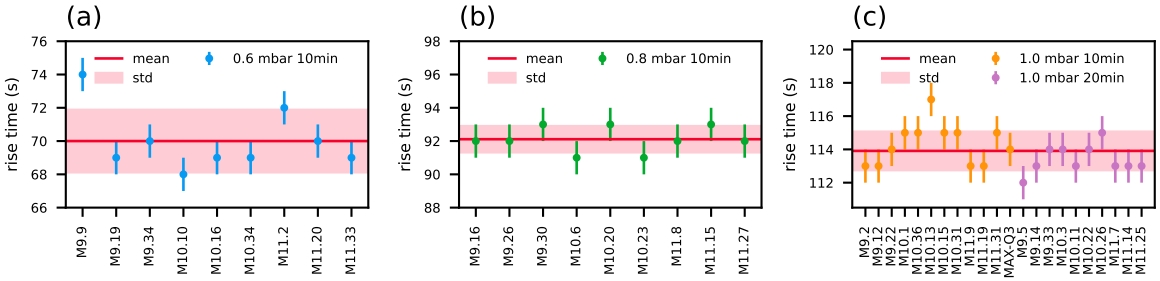

Fig. 3.12 Rise time of the oxygen pressure to (a) 0.6 mbar, (b) 0.8 mbar and (c) 1.0 mbar for junction oxidation in the *Plassys* evaporation system. The mean and standard deviation across all samples is indicated in red.

measured pressure increases with the target pressure, the relative deviations are below 2%.

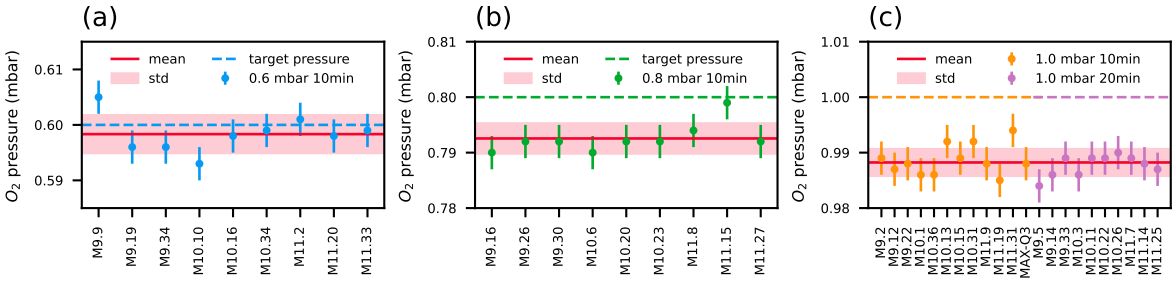

Fig. 3.13 Oxygen pressure measured for the individual samples. The dashed lines indicate the target pressure. In red the mean and standard deviation.(a) Pressure set to 0.6 mbar. (b) Pressure set to 0.8 mbar. (c) Pressure set to 1.0 mbar.

A set of junctions from a dose test was imaged using a scanning electron microscope (SEM) to obtain an average junction width. The junctions were fabricated at five different locations on the wafer. For each location two junctions with the same designed size were imaged. Fig. 3.14 shows a SEM picture for each junction size and the obtained mean width for the lower and upper electrode. The value in brackets is the average width assuming a square junction calculated from the area where lower and upper electrodes overlap. From now on I will refer to the junction width rather than the junction area as the width is what finally limited the fabrication. It is assumed that the different widths of the lower and upper junction electrodes come from the deposition of Al onto the resist mask causing it to become narrower. This is supported by the fact that the upper electrode is about 20 nm narrower than the bottom electrode, which matches the thickness of the bottom electrode. To confirm this a resist mask would have to be measured prior to evaporation. This has not been attempted yet as SEM imaging of resist is challenging. An alternative would be atomic force microscopy (AFM) imaging.

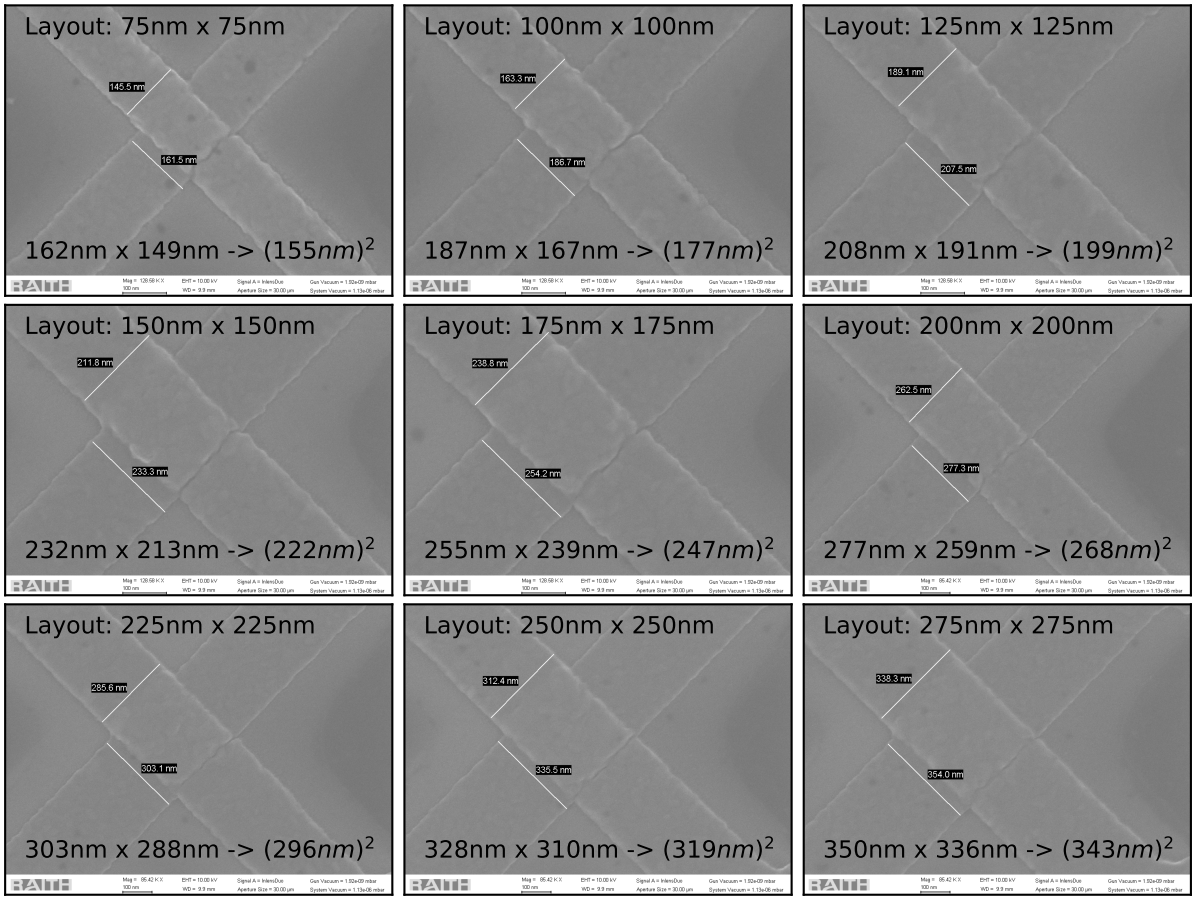

Fig. 3.14 SEM images of the nine different junction sizes with measurement markers. The black text at the top indicates the Layout width of the junctions. The black text on the bottom indicates the average width measured over multiple samples. The first value is for the bottom electrode, the second for the top electrode, and the third value is the average width calculated from the average area of the first two values assuming a square junction. The standard deviation in measurements are below 5 nm and assumed to result mainly from the accurate placing of the measurement markers.

CHAPTER 4

Normal State Resistance Measurements

In this chapter the measurement techniques to obtain the normal state resistance are discussed. Afterwards an explanation of the data treatment procedures is given. Finally the statistical results, obtained for the junction test devices, are discussed.

4.1 Automatic Probe Station

As the number of junctions in this thesis is quite large, probing resistance by hand was not an option. Instead an automatic probe station (*CascadeMicrotech CM300*) located at the *University of Innsbrucks Institute of Mechatronics* was used. The probe tips (*Picobrobe*) are made of tungsten and were specifically ordered for probing DC currents in Al thin films deposited on silicon or sapphire. The position of both tips can be set manually in all 3 dimensions. The sample is placed on a vacuum chuck that can be positioned by the control software with an accuracy of $0.2\,\mu$m. The machine uses a previously defined wafer map to drive the chuck relative to the tips in x,y and z direction. The only thing one has to do, is to align the rotation of the sample with the chuck, set the origin of the wafer map at the correct position of the sample and determine the contact height. The rest of the measurement can the be fully automated by a python script.

The probe station itself has no measurement device included thus a SMU (*Keysight B2912A*) was connected via *GPIB* to the machine. The probe tips are connected directly to the SMU by 1 m long wires with banana plugs. The python code triggers a measurement on the SMU once the probe station has reached a measurement position defined in the wafer map.

To improve measurement accuracy it was decided to probe every junction 5 times moving the probe tips by $5\,\mu$m in x direction between measurements. Due to the small size of the chips vacuum problems occurred that led to movement of the chips on the chuck. To circumvent this the chips were glued to a 4 inch Si wafer using *Crystalbond 555HMP*. In Fig. 4.1 this transfer

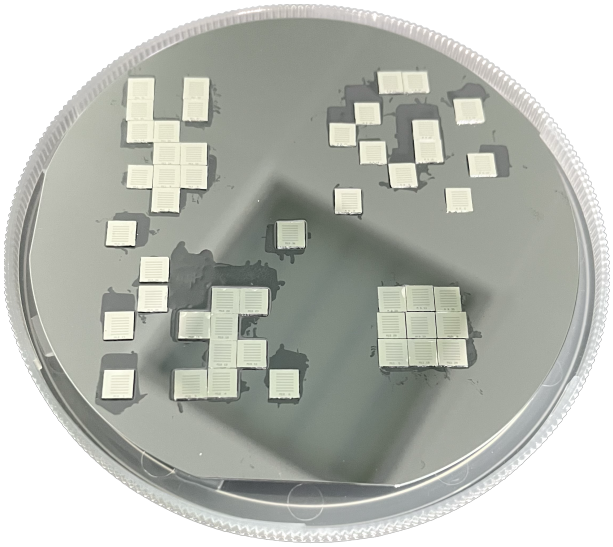

Fig. 4.1 Transfer wafer carrying the junction test devices. This is done to improve the vacuum suction on the automatic probe station.

wafer carrying the test devices is shown.

To get reliable resistance measurements it was decided to take voltage sweeps. Therefore a sweep of the voltage applied to the Junction from -0.1 to 0.1 V in 50 equal steps is performed. At every set voltage the actual voltage drop across the JJ and the current flowing through the junction is recorded. From this data the resistance can be obtained fitting it with Ohms law $I = V/R$.

4.2 Measurement Treatment

Before the statistical analysis the measurements of each chip have to be converted into resistance samples, that are cleared of systematic errors e.g. shorted or open junctions. For each I-V sweep measurement a resistance R_N^M is obtained. Values below 400 Ω are considered a short, the ones above 25 kΩ are considered an open. Open and shorts are discarded in further analysis. All other values, out of the five measurements per junction site, are then combined into a mean resistance $R_N^{\overline{M}}$.

One has to account for the finite resistance of the substrate and aluminum plane in parallel to the junction R_{PAR}, contributing $\approx 70\,\mathrm{k}\Omega$ in parallel. For every wafer 3 chips were stripped of the resist mask without an Al deposition, thus only containing probing pads and no junctions. The resistance was measured for each probe pad location with 5 I-V sweeps in the same way as the test junctions. For every pad position the mean over the three chips is then calculated. The junction resistance $R_N^{\overline{M}}$ is then corrected by

$$R_N^{\overline{M},p} = \left(\frac{1}{R_N^{\overline{M}}} - \frac{1}{R_{PAR}} \right)^{-1} \tag{4.1}$$

for the parallel resistance determined for the corresponding position and wafer. In Fig. 4.2(c) an example of a position resolved parallel resistance map is shown. The resistance tends to

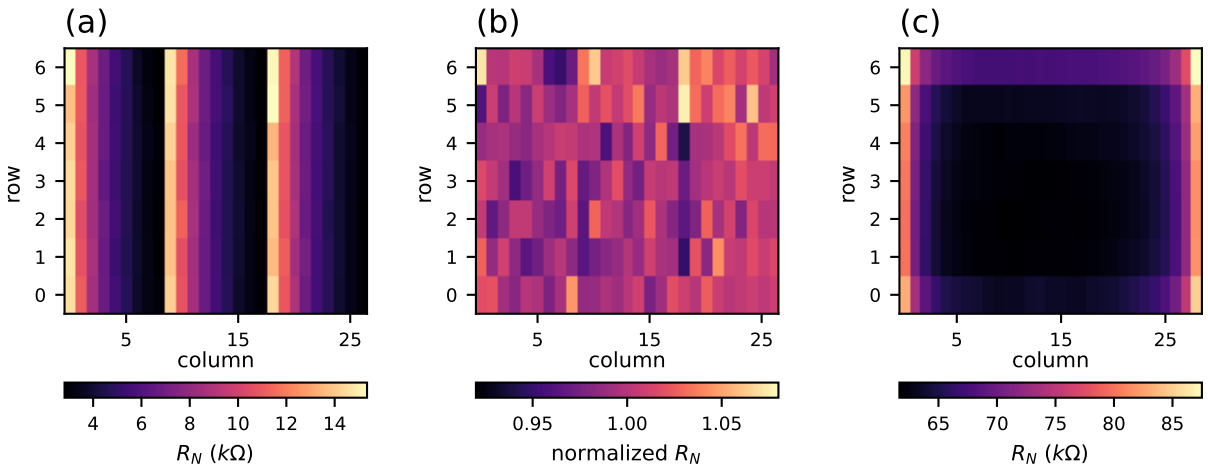

Fig. 4.2 Junction normal state resistance measurements. (a) Chip position resolved junction resistance. (b) Chip position resolved junction resistance normalized to the mean resistance of all same sized junctions on the chip. (c) Chip position resolved parallel resistance due to circuit and substrate.

increases with a radial symmetry from the center towards the edges. In the next steps it is ensured that errors for certain pad positions will not effect the statistic.

To correct the junction resistance for the offset resistance resulting from the wires of the measurement apparatus, the contact resistance, the pads and the junction electrodes, deliberate shorts were fabricated. One of these shorts is of the smallest and the other of the widest junction electrode size. The mean resistance value for both short sizes is calculated. Values below 50 Ω are considered a short, the ones above 400 kΩ are considered an open. Applying an interpolation a value for the other sized junctions is obtained, that corresponds to the change in resistance due to the varying electrode width. These values are then subtracted from the junction resistance $R_N^{\overline{M},p,s} = R_N^{\overline{M},p} - R_S$. This procedure is valid as the very thin electrodes induce more than 95% of the offset resistance. The probe tips and the wiring that do not change account for the other 5%.

Finally all junctions of a chip that have the same layout size are consider as one resistance sample. To ensure that no outliers effect the data analysis Chauvenet's criterion [45] is applied for every value in the sample

$$\operatorname{erf}\left(\left|\frac{R_N^{\overline{M},p,s} - \bar{R}_N}{\sqrt{2}\sigma_{R_N}}\right|\right) \geq 1 - \frac{1}{2N}, \tag{4.2}$$

where erf is the error function, $\bar{R}_N$ is the mean of the sample, σ_{R_N} is the standard deviation of the sample and N is the number of values in the sample. For N=21 this means a value more than 2.26σ away from the mean is considered an outlier. If an outlier is found Chauvenet's criterion is re-applied on the new sample with reduced N. Results R_N that pass Chauvenet's criterion are then used in the following statistical analysis. In Fig. 4.2(a) the position resolved junction resistance R_N for a test device chip is shown.

4.3 Analysis and Statistics

In this section the results from the resistance measurements will be analyzed. This can be done on three different levels. On chip, on wafer and globally over all three wafers. The test devices have been measured as soon as possible, latest within one week after fabrication.

4.3.1 On chip statistics

First, the on chip reproducibility is analyzed. The fabrication yield is defined as the fraction of junctions that made it into the final sample. Fig. 4.3(a) shows the mean yield dependent on junction width. There is no significant correlation between junction width and yield observable. The average fabrication yield over all sizes is 96%. This yield includes all junctions fabricated. As a remark it should be mentioned that the 96% yield justifies the use of Chauvenets's criterion, one expects about 5% of all values being outliers for 2σ. The yield is also influenced by junctions that were scratched off the chip due to the delicate handling of the small chips and could thus be higher. Chauvenets's criterion will also take care of chips that are off due to a error in the determined parallel resistance.

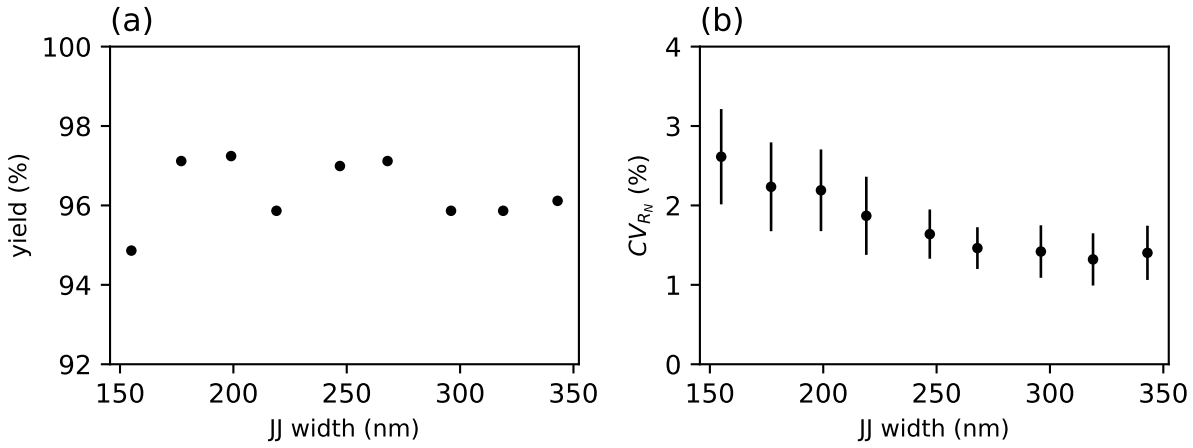

Fig. 4.3 On chip reproducibility for different junction sizes. (a) Average fabrication yield vs junction width. (b) Average coefficient of variance of the normal state resistance vs junction width.

The coefficient of variation is defined as the relative standard deviation $CV = \sigma_{R_N}/\bar{R}_N$. In Fig. 4.3(b) the average on chip CV_{R_N} is shown dependent on the junction width. One can observe higher CV_{R_N} for smaller junction widths. This can be explained by the relative change in junction area due to a variation in junction width being bigger for small junction widths. The same argument has to be considered for the edge line roughness of the junction boundary. Additionally the reader should be reminded that the smallest widths are the most challenging to fabricate due to the high aspect ratio in combination with the resolution of the e-beam system.

Besides the junction width the oxidation parameters have been varied. The different junction sizes can be compared by normalizing each junction to the mean of the related sample. Fig. 4.4 shows histograms of the normalized resistance for the four different oxidation parameters. The average standard deviation of the histograms is 3%. There is no set of evaporation parameters

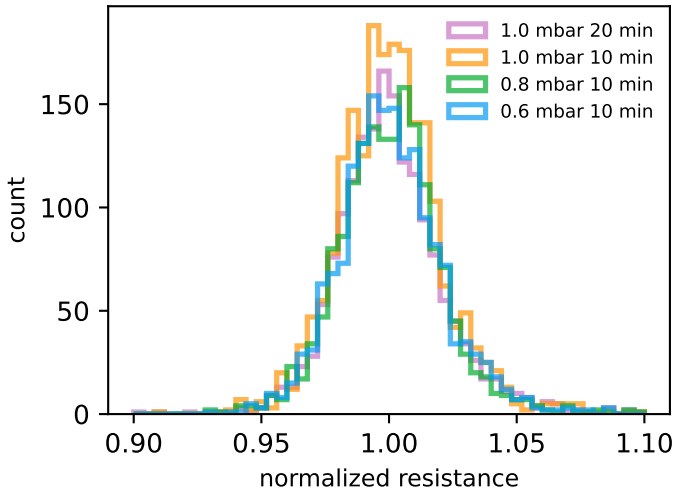

Fig. 4.4 Histograms of the on chip normalized resistance for different oxidation parameters. The histogram contains all chips used for the statistics section of the thesis. A value of 1 indicates a junction lies within the mean resistance of the same sized junction on the chip. The average standard deviation is 3%.

that would be favourable. An exemplary position resolved map of the normalized resistance of a test device is shown in Fig. 4.2(b). From this map no positional dependent variance can be observed.

4.3.2 On Wafer Statistics

In this section resistance samples on the same wafer will be combined. In Fig. 4.5 the average CV_{R_N} on a wafer is shown dependent on the junction width. For this, all resistance samples from the same wafer and with the same layout size and oxidation parameters have been combined to calculate a mean, standard deviation and CV_{R_N}. Then the average CV_{R_N} for different oxidation parameters is determined. As for the on chip statistics a correlation between smaller junction width and higher CV_{R_N} can be observed. Wafer M9 has in general a higher CV_{R_N} compared to wafer M10 and M11. The average on wafer CV_{R_N} is also higher than the average on chip CV_{R_N}.

In Fig. 4.6 histograms of the normalized resistance for each wafer and oxidation parameter is shown. Every chip sample is plotted separately, this way the contribution of the different chips to the mean resistance is better visible. One can observe that for some histograms there are chip samples that do not align with the normalized resistance of the other chips in this sample. This explains the in general higher CV_{R_N} for the on wafer statistics. For wafer M9 this deviation is especially high. The chips from wafer M11 fabricated with the oxidation parameters $p_{ox} = 1.0\,\mathrm{mbar}$ and $t_{ox} = 20\,\mathrm{min}$ align especially well with a standard deviation of 3%. Considering their individual position on the wafer (Fig. 3.10) they have been close together. The standard deviation is smaller as on the two chips of M10 that have been evaporated together which have a combined standard deviation of 4.8%. This hints that the resist mask has variations over the scale of multiple chip sizes, but more samples would be required to draw a statistically relevant conclusion. Such variations could result from a drift in beam current that would result

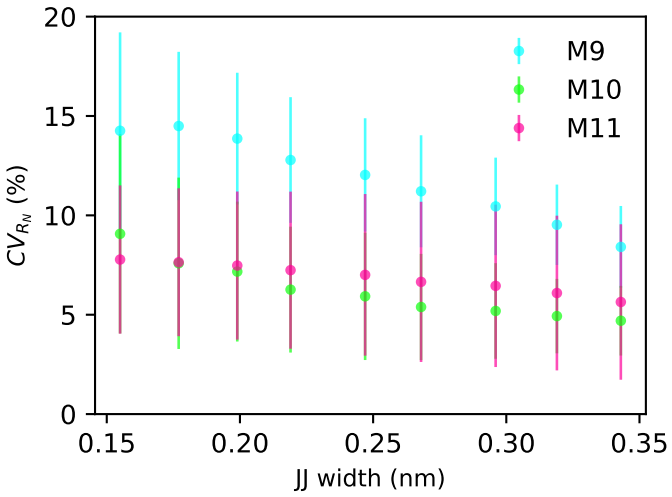

Fig. 4.5 On wafer reproducibility for different junction sizes. Average coefficient of variance for the normal state resistance of the different junction sizes.

in a different exposure dose, insufficient focus correction or inhomogeneous development. It is speculated that small variations in the resist film thickness should not influence the required exposure dose significantly enough. To rule this out as a source of spread further tests would have to be done.

4.3.3 Global Statistics

Combining samples globally over all wafers will include the spread that comes from completely separated fabrication runs. In Fig. 4.7 the average global CV_{R_N} is shown, dependent on the junction width. The values are comparable to the on wafer spread. The junction width dependence is clearly visible.

In Fig. 4.8 histograms of the normalized resistance for each oxidation parameter set are shown in solid. The lines indicate the contributions of the different wafers. The average global standard deviation is 10% and is dominated by the on wafer spread. It is claimed that there is still no preferred oxidation parameter that would yield lower spread. This leaves the conclusion that the reproducibility is limited by lithography or development. A significant correlation with the chip aging between fabrication and measurement could not be determined, as other variation sources are predominant.

From the global mean of samples with same size and oxidation parameters a standard parameter set can be defined to predict future fabrication. In Fig. 4.9(a) the global mean of the normal state resistance for different oxidation parameters is shown compared to the different junction widths. The error bars represent the standard deviations. Each parameter set is fitted with a junction width dependent resistance model $R_N = R_J/(d - \Delta d)^2$, with the condition that Δd is a global variable for all four fits. This Δd is an offset for the considered junction widths, that have been determined by SEM imaging for a set of test junctions and is just below $-1\,\mathrm{nm}$. The unit-area resistance R_J is determined separately for each curve as it depends on the oxidation

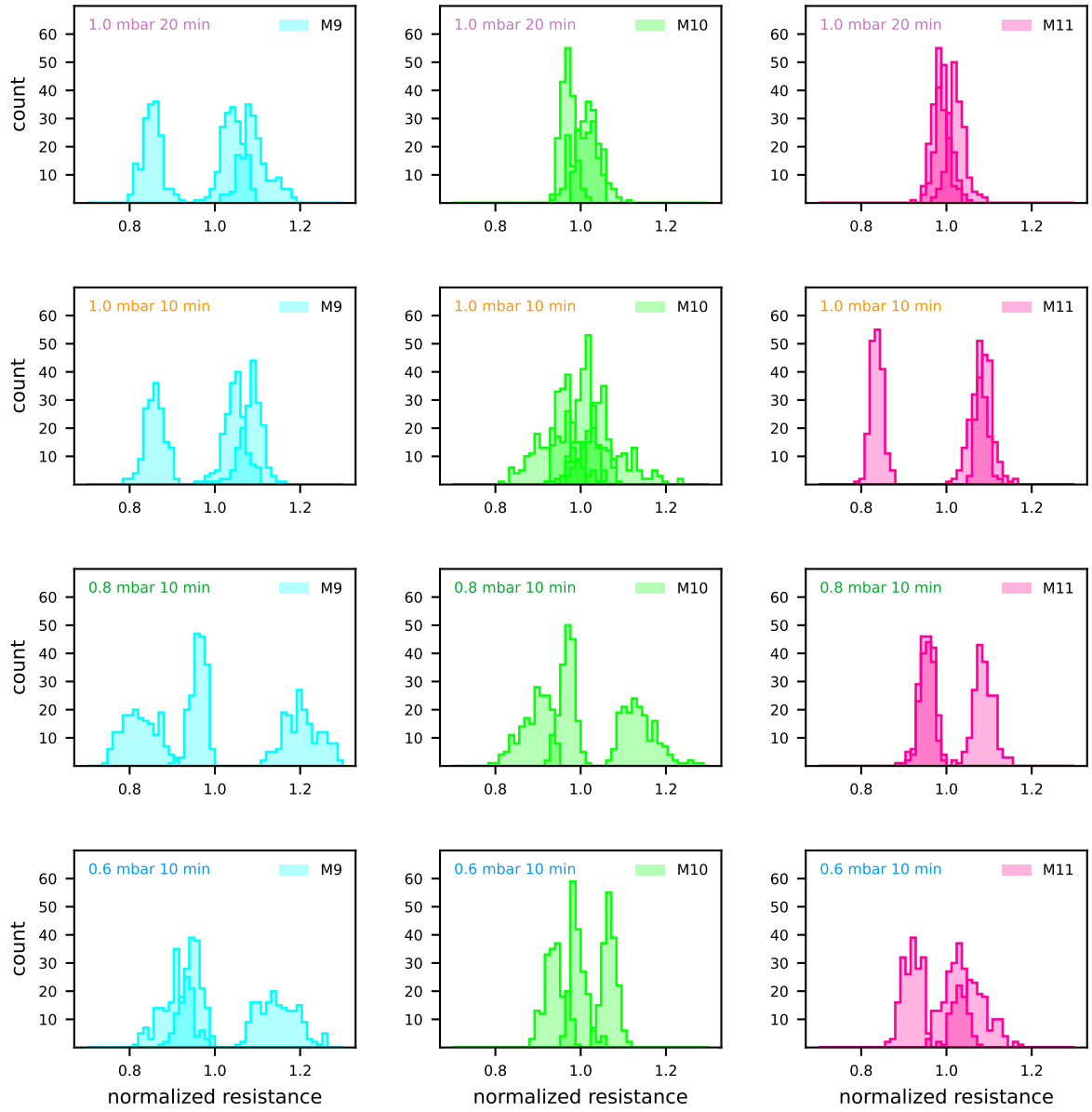

Fig. 4.6 Histograms of the on wafer normalized resistance for different oxidation parameters and wafers. The histograms in each figure are plotted separately for each chip, thus the color becomes more visible where chips overlay. A value of 1 indicates a junction lies within the mean resistance of the same sized junction on the wafer.

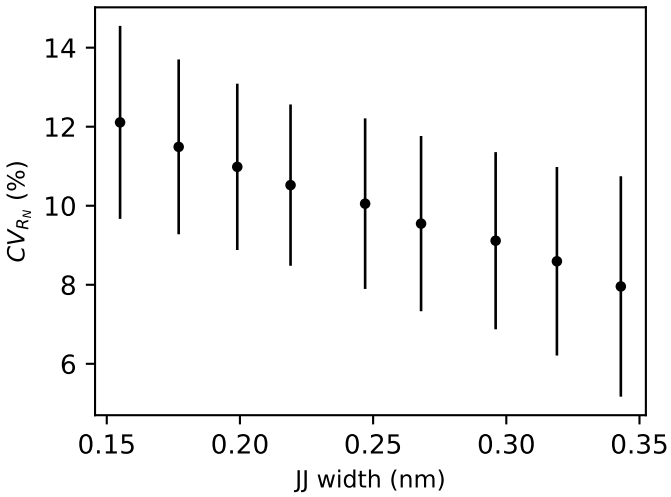

Fig. 4.7 Global reproducibility for different junction sizes. Average coefficient of variance for the normal state resistance of the different junction sizes.

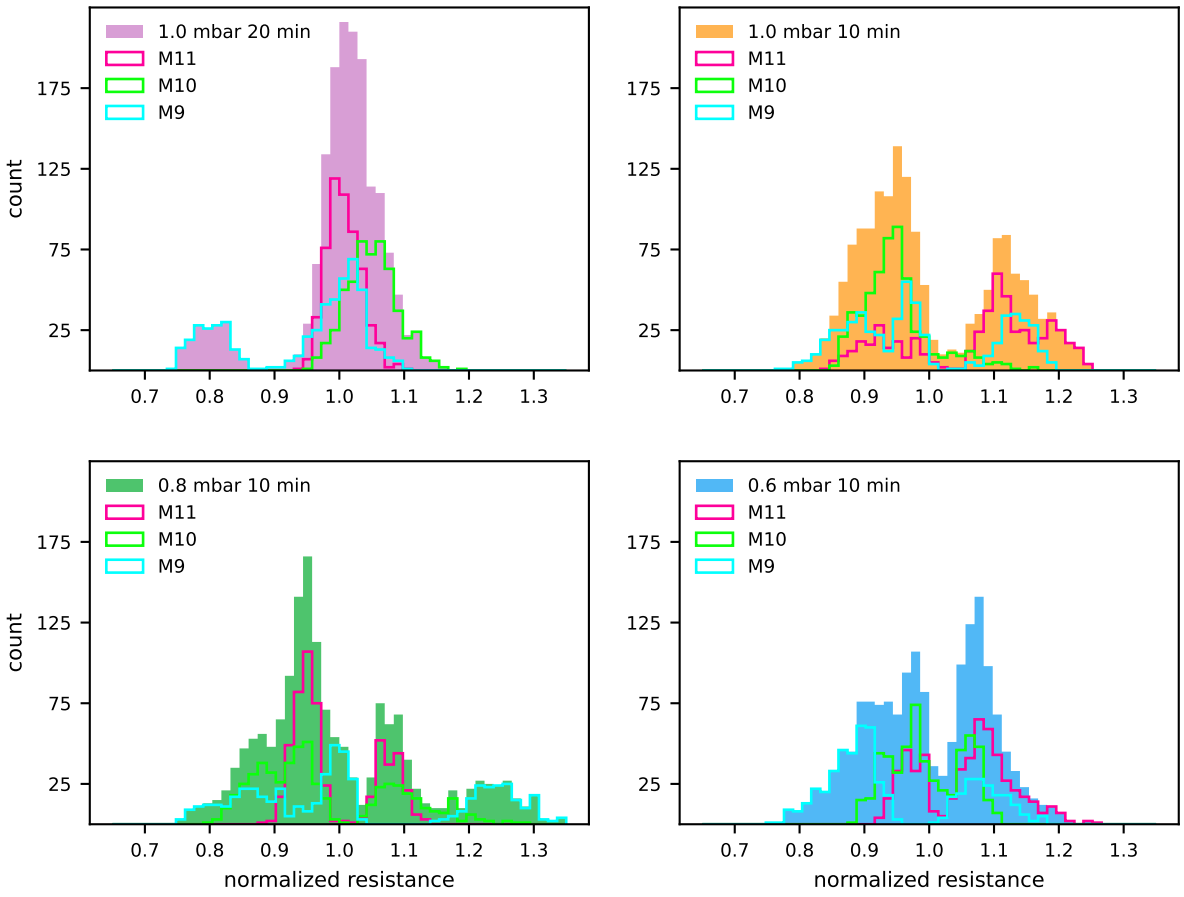

Fig. 4.8 Histograms of the global normalized resistance for different oxidation parameters and wafers. The filled histogram shows all samples together. Lines represent the contributions of samples from different wafers.

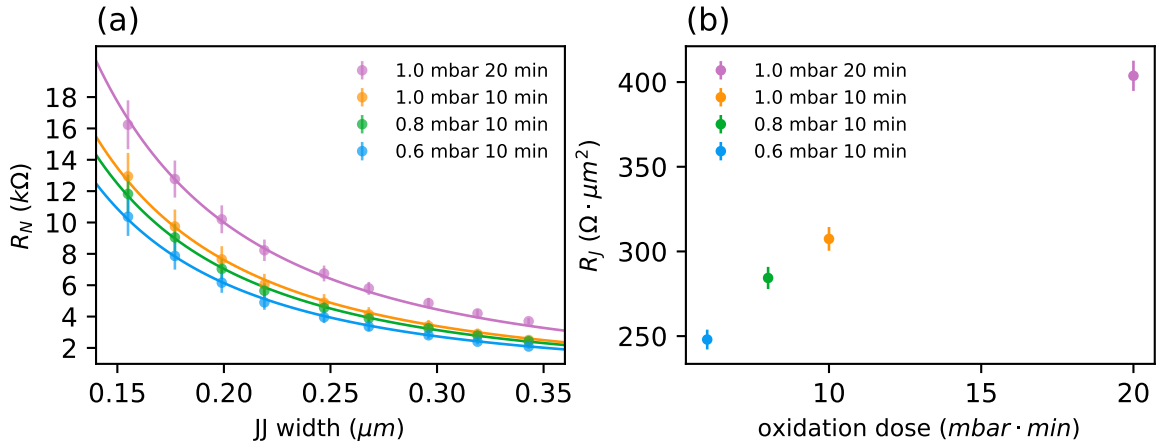

Fig. 4.9 Normalstate resistance. (a) Global normalstate resistance of different junction sizes for four different oxidation parameters. Each oxidation set has been fitted with an area dependent resistance law and a global junction size offset. (b) Unit-area resistance vs oxidation dose obtained from the fit in (a). Error bars represent standard deviation of the samples.

parameters. In Fig. 4.9(b) R_J is shown dependent on the oxidation dose ($p_{ox} \cdot t_{ox}$). It is clearly visible that R_J increases with the oxidation dose as expected. As a remark it has to be said that the rise time for the oxygen pressure and the time it needs to pump the chamber back to evaporation pressure are neglected here. The influence of p_{ox} and t_{ox} on R_J will most likely not be the same but it would require more data points to determine a qualitative model. The relation between R_J and oxidation dose is considered machine and material specific. In Ref. [41] a detailed study of oxidation dose has been carried out.

CHAPTER 5

X-mon Qubits

To validate the results obtained for the junction test devices X-mon qubits [18], a qubit based on the planar transmon qubit [19], were fabricated. In the following a brief introduction into the theory of transmon qubits is given. The rest of the chapter discusses the design, fabrication, and simulation of these qubits.

5.1 Theory

Superconducting qubits can be best explained by starting with an LC resonant circuit also known as a microwave resonator. A circuit diagram is drawn in Fig. 5.1(a). The energy in such a circuit is oscillating between the inductance L_r and the capacitance C_r. Quantisation of the lumped elements leads to the quantum harmonic oscillator (QHO) [6, 46]. The Hamiltonian of a LC QHO is given by

$$\hat{H} = 4E_{C_r}\hat{n}^2 + \frac{1}{2}E_{L_r}\hat{\phi}^2, \tag{5.1}$$

and includes the quantum operators, reduced charge $\hat{n} = Q/2\mathrm{e}$ and superconducting phase $\hat{\phi} = 2\pi\Phi/\Phi_0$. Here Φ denotes the flux through the inductor. $E_{C_r} = \mathrm{e}^2/(2C_r)$ is the charging energy to add an electron to the superconducting island. $E_{L_r} = (\Phi_0/2\pi)^2/L_r$ is called the inductive energy of the circuit. The quadratic potential of a QHO is shown in Fig. 5.1(b). One can write down the QHOs Hamiltonian in the form of second quantization by replacing $\hat{n}$ and $\hat{\phi}$

$$\hat{H} = \hbar\omega_r\left(\hat{a}^\dagger\hat{a} + \frac{1}{2}\right), \tag{5.2}$$

where the energy levels for a number of excitations $n = \hat{a}^\dagger\hat{a}$ are equidistantly spaced by the resonant frequency $\hbar\omega_r = \sqrt{8E_L E_C}$ of the system.

Due to the linear nature the QHO cannot be used as qubit. One needs to be able to define a computational subspace and thus needs energy levels with unique transition frequencies. Non-linearity can be achieved by substituting the inductor with a Josephson junction (Fig. 5.1(c)).

This circuit is commonly known as transmon qubit [19]. The Hamiltonian of a transmon will take the form

$$\hat{H} = 4E_{C_\Sigma}\hat{n}^2 - E_J \cos\left(\hat{\phi}\right), \tag{5.3}$$

where E_{C_Σ} takes into account the combined capacitance $C_\Sigma = C_J + C_S$ of Josephson junction and shunt capacitance respectively. The Josephson energy E_J was already introduced in chapter 3, Eq. 3.4. This Hamiltonian has a cosinusoidal potential as shown in Fig. 5.1(d). Using Taylor expansion of the cos part and making use of the rotating wave approximation one can write down the Hamiltonian in second quantization

$$\hat{H} = \hbar\omega_{01}\hat{b}^\dagger\hat{b} - \frac{E_C}{2}\hat{b}^\dagger\hat{b}^\dagger\hat{b}\hat{b}. \tag{5.4}$$

One can see that the different energy levels are no longer equidistantly spread. Solving the eigenvalue problem gives the eigenenergies

$$\hbar\omega_{01} = \sqrt{8E_J E_C} - E_C \tag{5.5}$$

for the ground to the first excited state and

$$\hbar\omega_{12} = \sqrt{8E_J E_C} - 2E_C \tag{5.6}$$

for the transition between the first and second excited state.

In general a Josephson junction by itself has a nonlinear inductance and a capacitance. But for a transmon qubit the ratio E_J/E_C should be above 40 to avoid charge sensitivity. This is called the transmon regime [19]. Thus the junction is shunted by a large capacitance. The anharmonicity is defined as the energy difference between the two exited states $\alpha = \omega_{12} - \omega_{01} = -E_C/\hbar$. In case of a transmon qubit anharmonicity equals the charging energy.

Coupling the transmon to a waveguide the resonance frequency $f_{01} = \omega_{01}/2\pi$ and the second qubit transition $f_{12} = \omega_{12}/2\pi$ can be revealed by microwave transmission measurements. Hence anharmonicity and thus E_C are known from the microwave measurements. The reader is referred to Ref. [47] for a detailed discussion of the coupling between qubit and waveguide. Knowing E_C one can calculate E_J solving Eq. 5.5

$$E_J = \frac{(\hbar\omega_{01} - E_C)^2}{8E_C}. \tag{5.7}$$

The effective superconducting gap Δ_{eff} can then be obtained

$$\Delta_{eff} = E_J R_N 8\mathrm{e}^2, \tag{5.8}$$

making use of Eq. 3.6 and Eq. 3.4.

Assuming variations in E_C are negligible the spread in f_{01} is about half of the spread in R_N. For a derivation the reader is referred to Ref. [48]. Only if CV_{R_N} is approaching 1%, lower variations in E_C will start to contribute significantly to the spread in f_{01} [11].

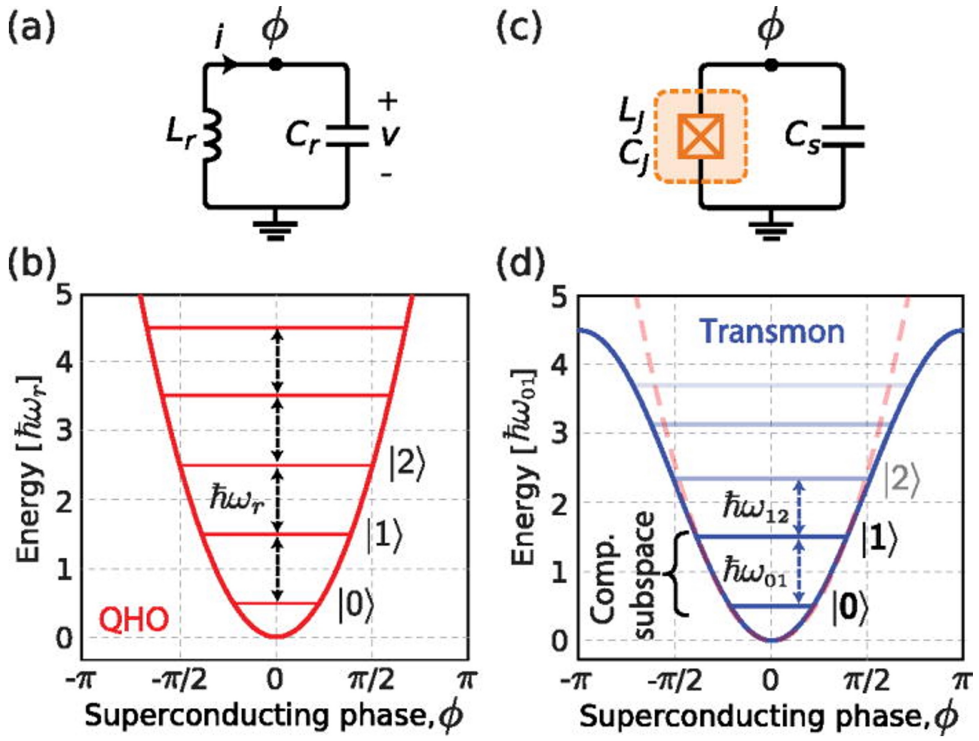

Fig. 5.1 (a) Circuit diagram of a quantum harmonic oscillator (QHO). (b) Energy level diagram of a QHO. (c) Circuit diagram of a transmon qubit, where the inductance of the QHO is replaced by a Josephson junction. (d) Energy level diagram of a transmon qubit. Figure taken from [6].

5.2 Design

Comparing the spread in room temperature test junction resistance to the spread in the qubits resonance frequencies allows to validate the room temperature measurements. Furthermore the effective gap Δ_{eff} is needed to predict the results of future fabrication. To suppress fabrication instability of elements other then the junctions the design was kept as simple as possible. The qubits are realized in form of planar fixed frequency X-mon qubits [18]. X-mon qubits are transmons with a ground reference. The shunt capacitance is realized between a cross shaped superconducting island and the ground plane. The junction is shunting the ground plane and its island as shown in Fig. 5.2. As the primary interest of the experiment is the resonant frequency, there are no readout resonators to determine the state of the qubits [8, 18, 19]. Instead the qubits are coupled capacitively to a coplanar waveguide or transmission line.

The size of the qubit chips was fixed at $1\,\mathrm{cm} \times 2\,\mathrm{cm}$ as sample boxes of this size were available. Each sample box has four SMA ports accommodating two transmission lines on a chip. As nine junction sizes were tested at room temperature and it was aimed to test all of these in qubits, nine qubits got coupled to each transmission line. Having different junction sizes also helps to correctly match resonant frequencies to qubit location when measuring R_N. The fabrication layout for a qubit chip is shown in Fig. 5.2. The distance between neighboring qubits was maximized to avoid coupling, while restricting the design to a straight transmission line for ease of fabrication. The transmission lines widen up at both ends to form bonding pads. The final

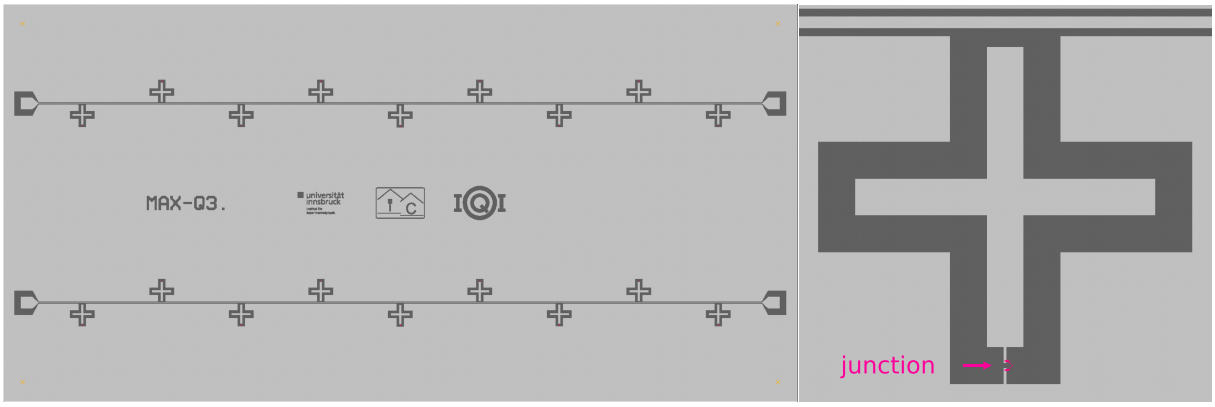

Fig. 5.2 Fabrication layout for a X-mon qubit chip. The 1 cm × 2 cm chip consists of two transmission lines that open up to a bonding pad at each end of the line. The X-mons qubits consist of a cross shaped capacitance that is shunted by a Josephson junction. The outer shape of the capacitance is build by the ground plane. The X-mon is capacitvely coupled to the transmission line.

size of the X-mon capacitance and coupling to the transmission line was obtained by simulation. It was decided to keep position and size of the cross the same for all qubits to limit simulation time and enable determination of the junction capacitance. A wafer fits three qubit chips, next to which six junction test devices (QT) are fabricated.

5.3 Simulation

Simulation of the qubits is necessary to determine the correct shunt capacitance and coupling to the transmission line. The dimensions of the transmission line had to be simulated so that the impedance is as close as possible to 50 Ω. This will ensure the transmission spectrum will not be limited by reflections. Simulations were performed using *Sonnet*.

When choosing E_C one has to ensure that the transmon regime $E_J/E_C > 40$ is reached. On the other hand the qubit resonant frequencies (Eq. 5.5) have to be supported by the microwave setup. Therefore resonant frequencies were limited from 3.5 GHz to 12 GHz. Solving these two considerations for a minimum qubit frequency of 3.5 GHz and $E_J/E_C = 80$ results in $E_J \approx 11.5\,\text{GHz}$ and $E_C \approx 0.14\,\text{GHz} \equiv 134\,\text{fF}$. The coupling of the qubit to the transmission line is linked to the dissipation. A too strong coupling will result in broad and shallow resonances in the transmission spectrum that at some point vanish. A weak coupling leads to a narrow resonance that is harder to find until the qubit does not couple anymore and no information can be gained. Thus as a compromise a coupling of 1 MHz was targeted.

Sonnet does not support nonlinear inductance such as Josephson junctions, thus qubits are modeled as an LC resonator. This will result in a resonance frequency E_C higher than the qubits resonance frequency. For simulation the vacuum, substrate and metallic planes of the qubit and transmission line are drawn. The junction is substituted by a lumped element capacitor and a linear inductor. To obtain an idea of the relation between cross size, cross gap and capacitance as well as distance to the transmission line and coupling to the transmission line, a single qubit of the lowest and highest frequency was simulated. In Fig. 5.3(a) the electrical currents found

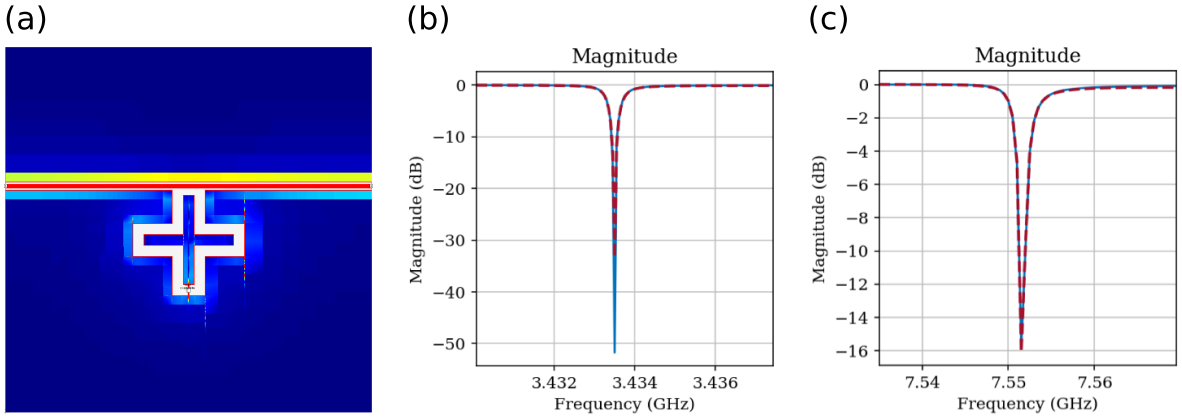

Fig. 5.3 Sonnet simulations of the X-mon qubit showing (a) the electrical currents, (b) the circle fit of the magnitude for a low frequency qubit and (c) the circle fit of the magnitude for high frequency qubit. In (a) blue corresponds to the lowest and red to the highest currents.

by a simulation are shown. At the time of the simulations the exact junction parameters from the RT devices were not yet known. Junctions were estimated to $C_J = 2.25\,\mathrm{fF}$, $L_J = 14.9\,\mathrm{nH}$ for the low and $C_J = 12.25\,\mathrm{fF}$, $L_J = 2.9\,\mathrm{nH}$ for the high frequency qubit. The simulations output is a S_{21} transmission spectrum. This data can then be processed by a circle fit routine. For an explanation of the circle fit procedure the reader is referred to Ref. [49, 50]. The simulations resulted in a cross of width $60\,\mu\mathrm{m}$ and length $490\,\mu\mathrm{m}$. The gap around the cross was set to $60\,\mu\mathrm{m}$ and the distance between the transmission lines central conductor and cross edge to $30\,\mu\mathrm{m}$. For the low frequency qubit (Fig. 5.3(b)) the final design resulted in a frequency of 3.43 GHz and a coupling of 0.4 MHz. The high frequency qubit (Fig. 5.3(c)) was at 7.55 GHz and was coupled with 1.9 MHz. Knowing the resonance frequency, set capacitance and inductance for the junction one can calculate the capacitance of the cross from Eq. 5.5. For the simulation $C_S = 142\,\mathrm{fF}$ and $C_S = 141\,\mathrm{fF}$ respectively was obtained, satisfying the two considerations from the beginning of this section.

5.4 Qubit Fabrication

Qubits are fabricated on Piranha etched Si prime wafers. A 100 nm Al layer is deposited on the substrate right after Piranha cleaning. Alignment and dicing marks are fabricated out of niobium. The mask for the test device chips and junction circuit is then exposed in the e-beam making use of a *CSAR* resist mask. After development, the mask is O_2 plasma cleaned in the *Sentech* and hard baked before the Al is etched with *Transene Type A*. Resist is removed in *AR600-546* followed by an ultrasonic bath in IPA. The resist layer for the junction fabrication is spun immediately after the IPA bath to minimise contamination onto the substrate. The junctions are fabricated with the $p_{ox} = 1.0\,\mathrm{mbar}$ and $t_{ox} = 10\,\mathrm{min}$ parameter set. In Fig. 5.4 a microscope image of a fabricated X-mon is shown. Once the junction fabrication is finished a protective layer of PMMA is spin coated onto the wafer for dicing. The baking temperature for the resist is kept at 80 °C for 3 min to avoid unwanted junction annealing. The wafer is then glued to a copper stencil for two runs of laser dicing. After dicing, the chips are removed from the stencil by immersing it in H_2O at 80 °C. The protective resist is removed in acetone

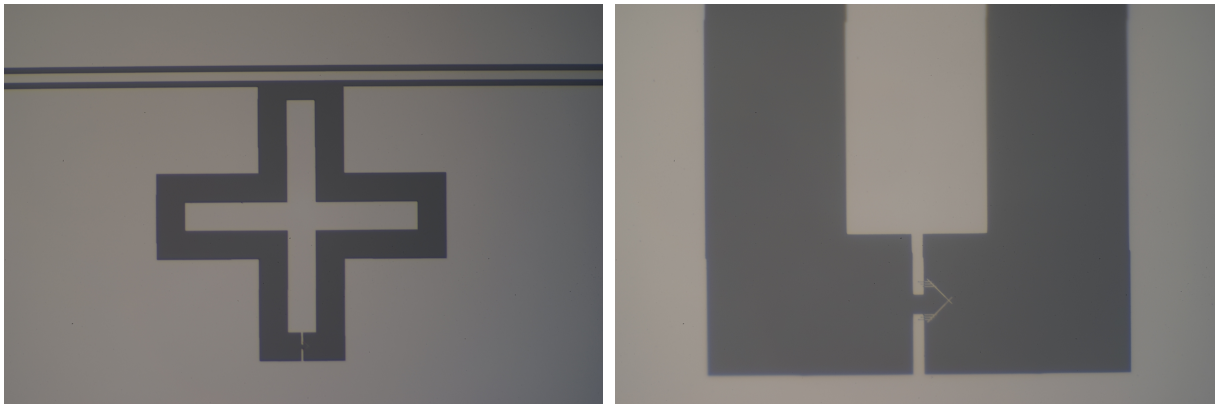

Fig. 5.4 Microscope image of a fabricated X-mon qubit. On the right picture the junction can be seen. The two cross arms of the qubit are 60 μm wide and 490 μm long.

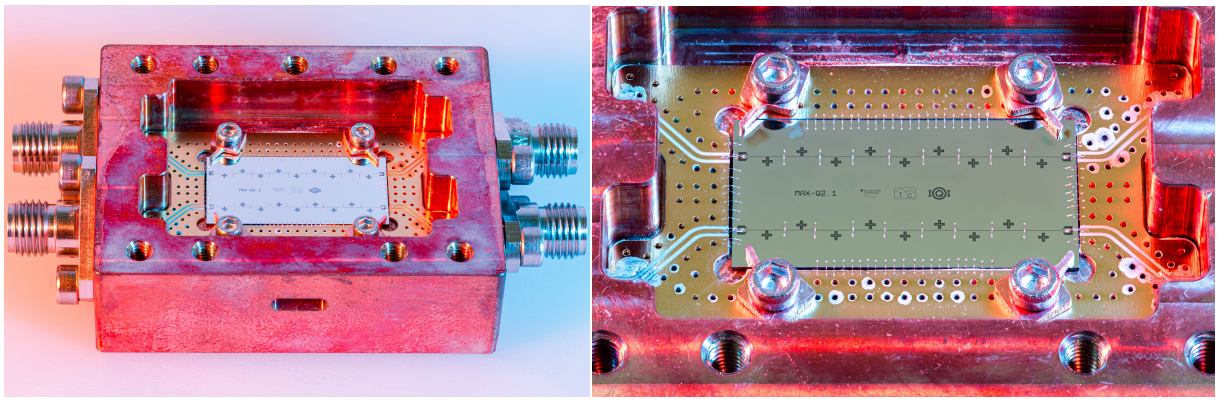

Fig. 5.5 Qubit chip in a copper sample box. The silicon chip in the center has a size of 1 cm $\times$ 2 cm. The SMA connectors are wired to the transmission line via PCB and wirebonds. Pictures taken and processed by David Jordan (IQOQI).

and IPA. The test device chips are then glued to a transfer wafer and probed on the automatic probe station. Qubit chips are clamped inside a sample box. The chip and the sample box PCB is connected through a 25 nm Al bonding wire. In Fig. 5.5 a qubit chip is shown inside the sample box. The sample box is closed with a copper lid for cooldown. One can see the wirebonds between the ground plane of the chip and the ground plane of the PCB. Additional wire bonds were placed over the transmission line to avoid spurious resonances on the ground plane. The chip from wafer MAX-Q2 shown in Fig. 5.5 was cooled down but due to a bug in initial simulations the qubits were to weakly coupled to measure a transmission. Wafer MAX-Q3 was then fabricated with the simulation results described in the section above. Chip MAX-Q3.1 and MAX-Q3.3 were mounted in the cryostat and the qubits were characterized.

CHAPTER 6

Qubit characterization

In this chapter the setup and techniques for the microwave measurements are described. An analysis of the obtained results is compared to the results for the junction test devices.

6.1 Cryogenic Setup

For the microwave measurements the sample box is mounted to the base plate of a dilution refrigerator. The *Oxford Instruments Triton* refrigerator reaches temperatures as low as 20 mK. These temperatures ensure the superconductivity of the Al thin films and avoid qubit excitation due to thermal radiation $\hbar\omega_{01} \gg k_B T$. In Fig. 6.1 a schematic of the microwave setup is shown. Generation and analysis of the microwave signals is performed outside the fridge indicated by the red and green box. The dashed lines indicate the different temperature stages of the refrigerator. Microwave signals entering the fridge are filtered and attenuated at different temperature stages to suppress thermal and electrical noise. The total attenuation of the input lines adds up to approximately 60 dB. On the base plate the input lines are connected to the sample via the SMA ports of the sample box. The signal travels through the transmission line on the chip interacting with the qubits before leaving the sample box on the other side. On the output lines the signal is amplified before it can be analyzed at room temperature. Amplification is provided by a high electron mobility transistor (HEMT) amplifier at the 4K stage and a second amplifier at room temperature. Isolators at the base plate connected the output lines protect the sample from thermal photons originating from higher stages.

6.2 Measurement Techniques

All microwave measurements presented in this thesis are transmission spectra using a vector network analyzer (VNA). The VNA is generating a microwave signal at its output that is then brought to interact with the system of interest before being fed back to its input. Comparing amplitude and phase of the input and output signal in a heterodyne detection scheme the

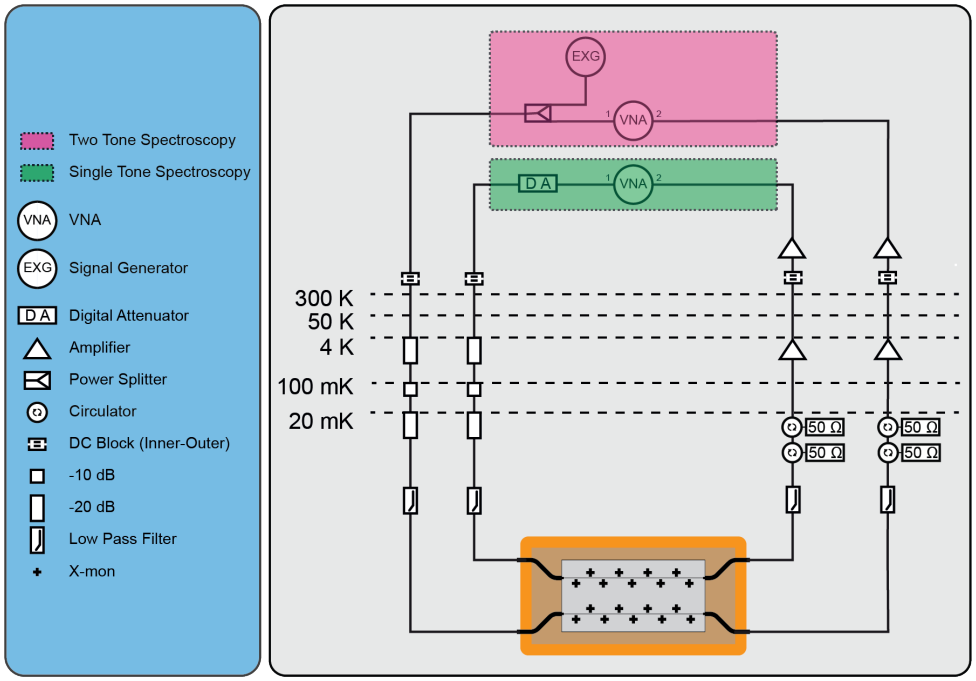

Fig. 6.1 Microwave setup for transmission measurements inside a dilution refrigerator. In green, single tone spectroscopy setup to obtain the resonance frequency f_{01} and quality factors of the qubit. In red two tone spectroscopy to probe the qubits second transition frequency f_{12}.

complex S parameters are determined. The transmission parameter S_{21} is the one of interest. Sweeping the frequency of the VNA output signal a transmission spectrum is obtained.

Qubit resonance frequencies f_{01} are determined by a single tone spectroscopy of the coupled transmission line. The setup is indicated by a green box in Fig. 6.1. A digital attenuator (DA) on the output side of the VNA is used to extend the range of signal power. If the VNA signal is in resonance with the qubit a dip in the transmission spectrum will occur due to destructive interference between VNA signal and signal reflected off the qubit [51]. An example is shown in Fig. 6.2 where a clear dip in magnitude $|S_{21}|^2$ at 7.378 GHz is visible. The power of the VNA signal has a strong influence on the dip. If the power is too high the qubit becomes saturated and the dip vanishes. For lower powers the dip becomes deeper and narrower. In addition to every low power measurement one at high power is taken for background subtraction. The data can then be processed with a circle fit routine to obtain the parameters of interest. To gain information about the dissipation channels of the qubits quality factors can be obtained from the circle fit. The higher the quality factor the longer the energy is stored in the qubit and thus dissipation is smaller. The internal losses of the qubit e.g. dielectric losses are described by Q_{int}. External losses Q_c depend on coupling to the transmission line resulting in leakage to the environment. The best estimate of the quality factors is obtained by probing the qubit with as low power as possible. The limitation is usually set by the signal to noise ratio (SNR) of the measurement. The SNR can be improved by averaging over multiple measurement traces.

The f_{12} transition of the qubit is only accessible if some population is in the first exited state. Only then one can drive population from there to the second excited state. A direct single

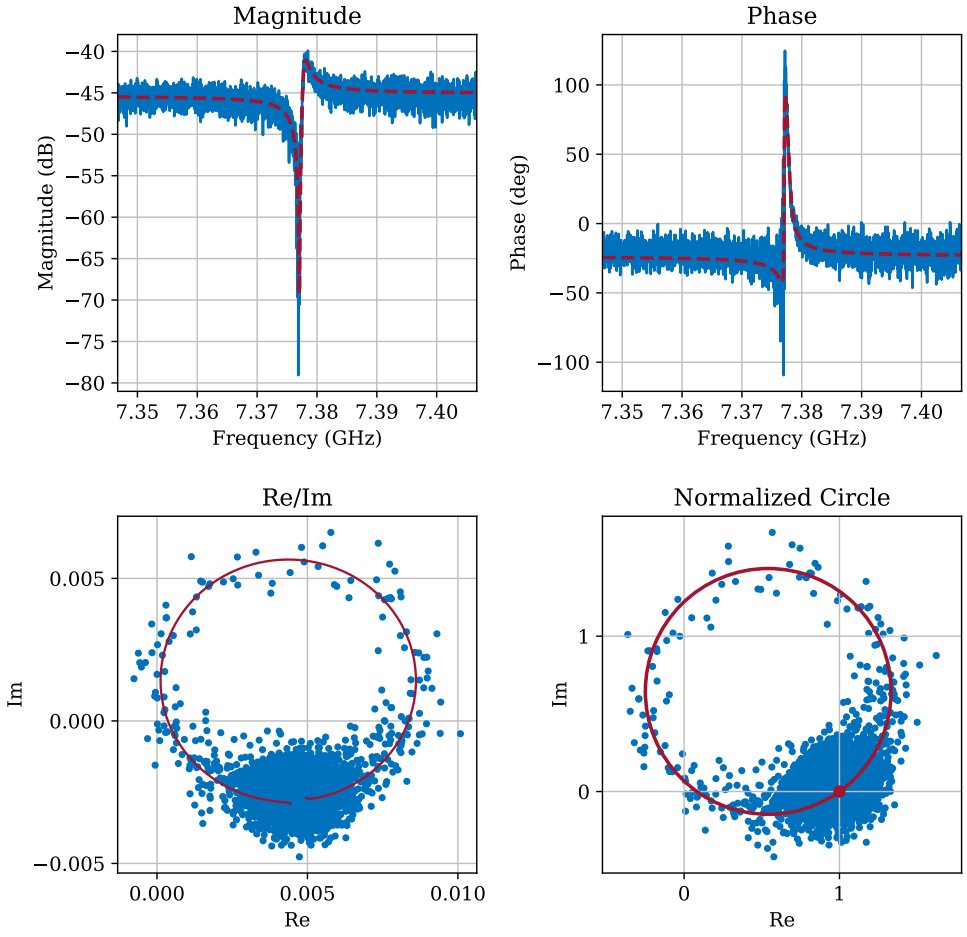

Fig. 6.2 S_{21} transmission spectrum with circle fit of the f_{01} transition of a X-mon qubit.

photon transition from the ground to the second excited state is forbidden. To populate the exited state a drive signal at the qubits resonance frequency has to be applied. Rule of thumb is that a 3 dB dip in transmission is equivalent to 50% population in the excited state. One speaks of two tone spectroscopy when driving the qubit at the f_{01} while performing a transmission measurement at the expected f_{12} frequency. The microwave setup for a two tone spectroscopy is indicated in red in Fig. 6.1. The VNA output signal is combined with a qubit drive from an external signal generator. In the $|S_{21}|^2$ transmission spectrum shown in Fig. 6.3 a dip for f_{12} and f_{01} occur. For a circle fit a separate narrower spectrum of the f_{12} transition is taken.

6.3 Results

Two qubit chips each containing two transmission lines with nine qubits were characterized during the cooldowns. Unfortunately, the second line on MAX-Q3.3 showed no transmission. The qubits of each chip are labeled Q1-Q9 with increasing frequency. Qubits from different

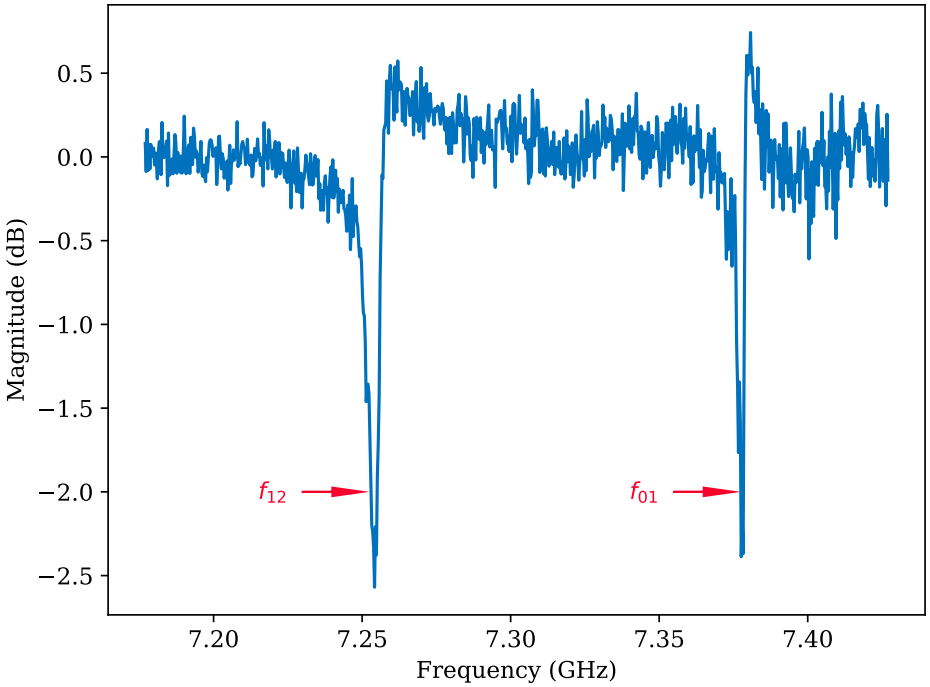

Fig. 6.3 $|S_{21}|^2$ transmission spectrum, showing f_{01} and f_{12} of a X-mon qubit. A pump tone was applied to the f_{01} transition to access the f_{12} transition. The difference of the two corresponds to the anharmonicity of the qubit.

transmission lines but the same Q label are fabricated with the same junction size. The normal state resistance of qubit junction test devices (QT) was measured during the time of the first cooldown. Data treatment was identical to the junction test devices with the exception of the parallel resistance treatment. As there were no extra chips without junctions every measurement considered an open was used to define a mean parallel resistance $\overline{R}_{PAR} = 66.959\,\mathrm{k\Omega}$. All resistance measurements have been corrected with this fixed value. The value seems plausible looking at the parallel resistances determined for the junction test devices. The mean R_N values and coefficients of variance are shown in Tab. 6.1. One QT chip has been excluded from the mean calculation as it was quite off from the other measurements. There was contact with the laser dicer nozzle during dicing at this chips location which may have damaged the substrate. Another explanation would be the position of the chip towards the edge where the resist thickness variations could form edge beads which could influence the lithography dose. It was also the last chip written in the lithography step so a drift of beam current could have occurred. A two inch wafer is also bigger then the *Plassys* evaporation crucible so directionality of the evaporation is not truly directional anymore as described in Ref. [43].

The qubits resonance frequencies f_{01} determined in the first cooldown are shown in Tab. 6.1. The coefficient of variation $CV_{f_{01}}$ is on average below 1.6%. Interestingly, it doesn't seem to scale with junction width anymore, but one would have to characterize more qubits to get a statistically significant conclusion. Unfortunately no qubits below 3.77 GHz could be characterized in the transmission measurements due to the filtering of the setup. For future experiments the lowest frequency should be targeted at 4 GHz or the filtering has to be adapted. In general R_N

was higher than assumed in the simulations, resulting in lower resonance frequencies.

An effective superconducting gap Δ_{eff} can be calculated for each measured f_{01} from Eq. 5.8. As the anharmonicity was not determined during the first cooldown the values determined during the second cooldown are used. The capacity of a qubit is not expected to change from ageing and thus neither does the anharmonicity. The mean calculated gap for related qubits is shown in Tab. 6.1. There seems to be a trend of increasing gap with the size of the junction that cannot be explain yet. The average effective gap obtained is $\Delta_{eff} = 154 \pm 15$ μeV. In Ref. [8] effective gaps of $150 - 200$ μeV are reported as common.

Tab. 6.1 Qubit parameters of first cooldown. $f_{01}^{3.1.1}$, $f_{01}^{3.1.2}$ and $f_{01}^{3.3.1}$ are the resonant frequencies determined for the respective qubit and transmission line. $CV_{f_{01}}$ is the coefficient of variance for the measured frequencies. $\overline{R}_N$ is the mean temperature resistance of the junction test devices with coefficient of variance CV_{R_N}. $\overline{\Delta}_{eff}$ is the mean effective superconducting gap calculated from the values in the table using E_C values determined during the second cooldown.

	$f_{01}^{3.1.1}$ (GHz)	$f_{01}^{3.1.2}$ (GHz)	$f_{01}^{3.3.1}$ (GHz)	$CV_{f_{01}}$ (%)	$\overline{R}_N$ (kΩ)	CV_{R_N} (%)	$\overline{\Delta}_{eff}$ (μeV)
Q1	-	-	-	-	13.5 ± 1.4	10.3	-
Q2	-	-	-	-	10.0 ± 1.0	9.7	-
Q3	3.826	-	3.773	1.0	7.7 ± 0.7	9.6	-
Q4	4.481	4.452	4.458	0.3	6.1 ± 0.4	6.4	135.7 ± 1.3
Q5	5.096	4.974	5.101	1.4	4.80 ± 0.27	5.7	139 ± 4
Q6	5.762	5.628	5.649	1.3	3.99 ± 0.22	5.4	154 ± 4
Q7	6.363	5.958	6.144	3.3	3.27 ± 0.17	5.3	153 ± 12
Q8	6.867	6.819	6.738	1.0	2.82 ± 0.14	5.0	166 ± 7
Q9	7.466	7.318	7.197	1.8	2.44 ± 0.14	5.8	175 ± 6

In Tab. 6.2 the mean values obtained for the second cooldown are shown. The aging from first to second cooldown of the qubits leads to a frequency decrease of an average $-1.3 \pm 0.2\%$. This shifted the two Q3 qubits measured during the first cooldown below the measurement range. The coefficient of variance $CV_{f_{01}}$ is on average still below 1.6%. From low power measurements internal quality factors Q_{int} of the qubits are obtained. The internal quality factors give information about the dissipation in the qubits. Quality factors are in the range of $10^4 - 10^5$. As the qubits are in the overcoupled regime these quality factors contain limited information due to Fano interference [52]. Overcoupled means that the dissipation due to the coupling Q_c to the waveguide is larger than the internal losses $Q_{int}/Q_c > 1$. The obtained Q_c is between 1000 and 10000 as expected for the targeted ± 1 MHz coupling, but these values are also effected by the Fano interferences. The anharmonicity of the qubits has an average coefficient of variance CV_α of 1%. In Fig. 6.4(b) the qubit capacitance $C_\Sigma = C_J + C_S$ calculated from $\alpha = -E_C$ is shown vs the area of the junctions. One expects the Junction capacitance C_J to increase with junction size. The data is fitted with a model $C_\Sigma = C_{J0} \cdot A + C_S$ and a shunt capacitance of $C_S = 106 \pm 2$ fF is obtained. The unit area capacitance of the junctions is determined to $C_{J0} = 422 \pm 26$ fF/µm^2. This value is high compared to 100 ± 25 fF/µm^2 that was found in Ref. [53]. The measured shunt capacitance is 20% smaller than the simulated one.

Tab. 6.2 Qubit parameters of second cooldown. $\overline{f}_{01}$ and $CV_{f_{01}}$ are the average qubit frequency and the respective coefficient of variance. $\overline{\alpha}$ and CV_α are the average anharmonicity and the respective coefficient of variance. $\overline{R}_N$ and CV_{R_N} are the average normalstate resistance and the respective coefficient of variance. $\overline{\Delta}_{eff}$ is the average superconducting gap determined from the values in the table. $\overline{Q}_{int}$ is the average inetrnal quality factor of the qubits.

	$\overline{f}_{01}$ (GHz)	$CV_{f_{01}}$ (%)	$\overline{\alpha}$ (MHz)	CV_α (%)	$\overline{R}_N$ (kΩ)	CV_{R_N} (%)	$\overline{\Delta}_{eff}$ (μeV)	$\overline{Q}_{int}$ 10^5
Q4	4.409 ± 0.016	0.4	-152.3 ± 0.6	0.4	5.95 ± 0.08	1.4	130.1 ± 1.1	0.21 ± 0.11
Q5	4.99 ± 0.06	1.3	-149.7 ± 3.1	2.0	5.7 ± 0.8	13.7	160 ± 21	0.9 ± 1.2
Q6	5.60 ± 0.08	1.4	-141.0 ± 0	0.0	4.06 ± 0.05	1.2	152 ± 4	0.18 ± 0.15
Q7	6.08 ± 0.19	3.2	-135.3 ± 2.3	1.7	3.46 ± 0.20	5.8	159 ± 21	0.53 ± 0.35
Q8	6.70 ± 0.07	1.1	-131.3 ± 3.2	2.5	2.91 ± 0.09	3.0	165.9 ± 3.3	0.15 ± 0.12
Q9	7.23 ± 0.15	2.1	-124.0 ± 0	0.0	2.52 ± 0.13	5.0	176 ± 8	0.4 ± 0.4

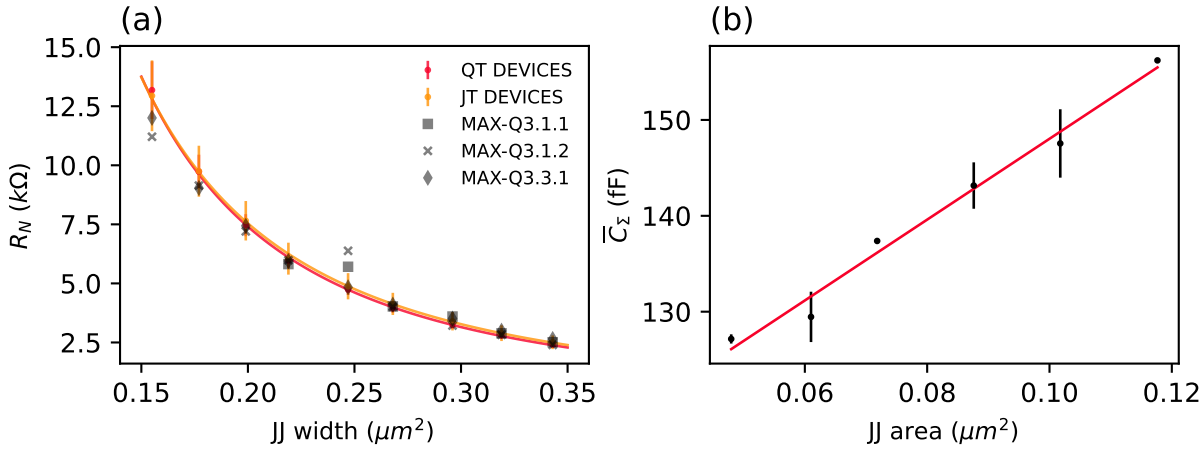

Fig. 6.4 Qubit parameters. (a) Normal state Resistance R_N vs junction width for qubits, RT devices and QT devices. Qubit R_N was measured after second cooldown while others devices were measured within a few days after fabrication. (b) Qubit capacitance vs junction area. A linear model is fitted to obtain the unit area capacitance. The fit results in a value of $C_{J0} = 422 \pm 26$ fF/µm^2.

The normal state resistance of each qubit was measured after the second cooldown with a single I_V trace. The values were corrected by the average short resistance from the QT devices and the same fixed value for the parallel resistance. The values are shown in Fig. 6.4(a) and mainly agree with the junction test devices (JT) and QT devices. One has to consider that the qubit resistance suffered from aging effects leading to increased resistance while JT and QT samples were measured within a few days after fabrication. Qubit chip MAX-Q1.1 broke during measurement right next to the junctions of Q5. It is expected that substrate edge effects lead to an increased resistance explaining the significant deviation from the other measurements. From Tab. 6.2 one can see that $CV_{f_{01}}$ is roughly half of CV_{R_N}. This yields that the junctions are still the main contributor to the variance of resonance frequency. For a statistically meaningful results more qubits would have to be fabricated.

The effective gap for each qubit from the parameters obtained during the second cooldown was calculated. The mean values are displayed in Tab. 6.2. The average gap over all qubits of the second cooldown is $\Delta_{eff} = 152 \pm 15$ μeV, which is in agreement with the first cooldown. For the calculation of this value the two qubits with increased R_N have been neglected.

CHAPTER 7

Conclusion and Outlook

During this thesis, fabrication of Manhattan style Josephson junctions was established for the first time in the *QNZT* cleanroom. Adopting the PICT process bandages can be fabricated in situ. Optimization of the fabrication parameters lead to a standard recipe for future fabrication on silicon substrates. Proximity error correction showed to be an important part in the optimization of the lithography.

The goal was to improve reproducibility and predictability of junction fabrication. Thus normal state resistance of nine different sizes and four sets of oxidation parameters have been characterized. A fabrication yield above 96% promises a reliable process. An average on chip standard deviation better then 3% could be achieved. The on wafer spread showed to be 10% in average. Only a single wafer showed 20% on wafer spread for the smallest junctions. Between 3 different wafers an average global spread of 10% was reached and it could be shown that this global spread is limited by the on wafer spread. In general the variation seems to scale with junction width which can be explained by the relative variations in junction area. The obtained spreads are a big improvement compared to previous fabrication results.

It is assumed that the on wafer spread is limited by lithography or development. Improvement could be achieved by further studies of the descum process [15]. Lithography is believed to be currently limited by the machine properties. If reproducibility is guaranteed, junction widths turned out to be bigger than the layout. It is an ongoing discussion in the community if bigger and thus better reproducible junction come at the cost of an increased TLS density [11]. A next step could be the evaporation of a complete wafer of test devices. A map of junction resistance in combination with SEM imaging could lead to further conclusions. Reproducibility of the oxide barrier growth seems to not be the limiting factor yet. Still it leaves room for improvement. The understanding of oxide growth is ongoing research [40–42]. Studies showed that evaporation parameters and resulting aluminum grain size influence the homogeneity of the tunnel barrier [15, 29]. With an update of the *Plassys* evaporation system, dynamic oxidation will be possible

[43, 44]. This has shown to further improve the homogeneity of the oxidation.

Characterization of X-mon qubits showed the operational capability of the junctions. The resonance frequency spread in qubits turned out to be below 1.6%. Considering that the qubits were fabricated over a whole wafer the spread was even lower than expected from junction test devices. An assumption is that the test device suffer from proximity effect as they are only spread by 100 μm and PEC has been done on the single junction, while the qubits are spaced by more than 2 mm. Direct measurement of qubit junction resistivity showed that the spread in resonance frequency is roughly half of the resistance spread. To give a finite conclusion about resonance frequency spread more qubits will have to be fabricated.

Determination of an effective superconducting gap in combination with the test devices will help with the resonance frequency prediction for future qubits. The barrier has only little influence on the gap that is set by the different thicknesses of the electrodes. Capacitance of the Manhattan junctions seems to be high. If shown to be correct, this is important knowledge for the simulation of new designs.

The next steps will be to include the new junctions into other experiments. For this the milling should be adapted for different circuit materials such as Niobium and Tantalum. A recipe to fabricate on sapphire substrates will have to be developed. This includes proximity error correction for the different material stack and the addition of a discharge layer. For a qualitative analysis of dissipation the qubit coupling has to be reduced. A more promising way is the introduction of readout resonators to measure coherence times T_1 and T_2. Fabrication of SQUID loops in the Manhatten geometry has yet to be tested [8] and a study of junction aging would further improve predictability.

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